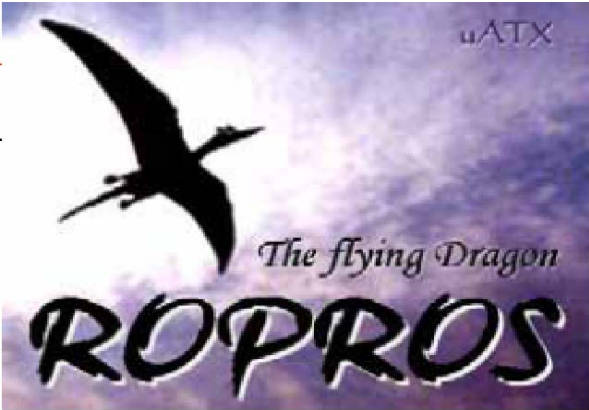


Ropros-E(Mate/VS) & Poseidon-E

MS-7428N1 Version 0B



MS-6619N1	ERP Number	Function
MS-7428-XX	601-7428-XXX	Mainboard
MS-4032-020 (MA)	604-4032-020	Front USB/ PWR BTN
MS-4142-010 (VS)	604-4142-010	Front USB/ PWR BTN

How to distinguish the different SKU

BLUE Color which mean all model need use

ORANGE Color which mean ROPROS-MA use

BROWN Color which mean the part reserve

PINK Color which mean ROPROS-VS (G45/G43)

Green Color which mean Poseidon-E

Model type	Function	BOM Config	ERP BOM No	BOM Opt.
MS-7428N1-xx	Eaglelake G43+ICH10+LPT+COM+TPM+KBMS for MATE.	CFG-MA	601-7428-XXX	
MS-7428N1-xx	Eaglelake G45+ICH10+F-USB2+KB+HD Audio+SYS FAN for VS.	CFG-VS_G45	601-7428-XXX	
MS-7428N1-xx	Eaglelake G43+ICH10+F-USB2+KB+HD Audio+SYS FAN+2DIMMs for VS.	CFG-VS_G43	601-7428-XXX	
MS-7428N1-xx	Eaglelake G45+ICH10R+F-USB2+KB+HD Audio+SYS FAN+6SATA for VS.	CFG-PSD	601-7428-XXX	

CPU:
Intel Yorkfield, Wolfdale,
Conroe, Conroe-1M, Conroe-L - 65W CPU
(FSB1333/1066/800)

System Chipset:
Intel EaglelakeG4X - GMCH (North Bridge)
Intel ICH10/ICH10R (South Bridge)

On Board Chipset:
Gigabit LAN - Broadcom BCM5784M
HD Audio Codec - Realtek ALC262 VD
LPC Super I/O : SMSC SCH5617
Clock GEN - IDTCV184-2
TPM - SLB 9635 TT1.2

Main Memory:
Dual Channel DDR II-800*4 (Up to 4GByte)

Intersil PWM:
VRD11 Intersil 6312 (3phase)

Expansion Slots:
PCI-E[X16] Slot *1
PCI-E[X1] Slot *1
PCI Slot *2

CONTENT	SHEET
Cover Sheet / Block Diagram	1-2
Intel LGA775 CPU - Signals / PWR / GND	3-5
Eaglelake - FSB / PCIE / VGA / MISC	6-7
Eaglelake - MEM_DDR2 / Power / GND	8-10
ICH10 - PCI / USB / DMI / PCIE	11
ICH10 - Host/ DMI/ SATA/ Audio/ SPI / RTC/ MSIC	12
ICH10 - Power / GND	13
DDR II - DIMM 1 / 2 / 3 / 4	14-15
Clock Generator - IDTCV184-2	16
SCH5617C / COM1&2 / FDD	17
CPU/SYS/PWR FAN	18
PCI-Express [X16] & [X1]	19
PCI Slot	20
USB Connector	21
VGA Connector	22
KB / MS / TPM / PARALLEL	23
Intersil-6312 (3Phase)	24
MS7 ACPI Controller	25
DIMM/GMCH Power (MS11)	26
ATX / Front Panal / SATA Connector	27
Broadcom - BCM5784M	28
HD Audio - ALC262	29
GPIO & Jumper Setting	30
Manual Parts	31
Power Distribution	32
PWROK Map & Reset Map	33-34
History	35

MSI

MICRO-STAR INT'L CO.,LTD

MS-7428N1

Size Custom

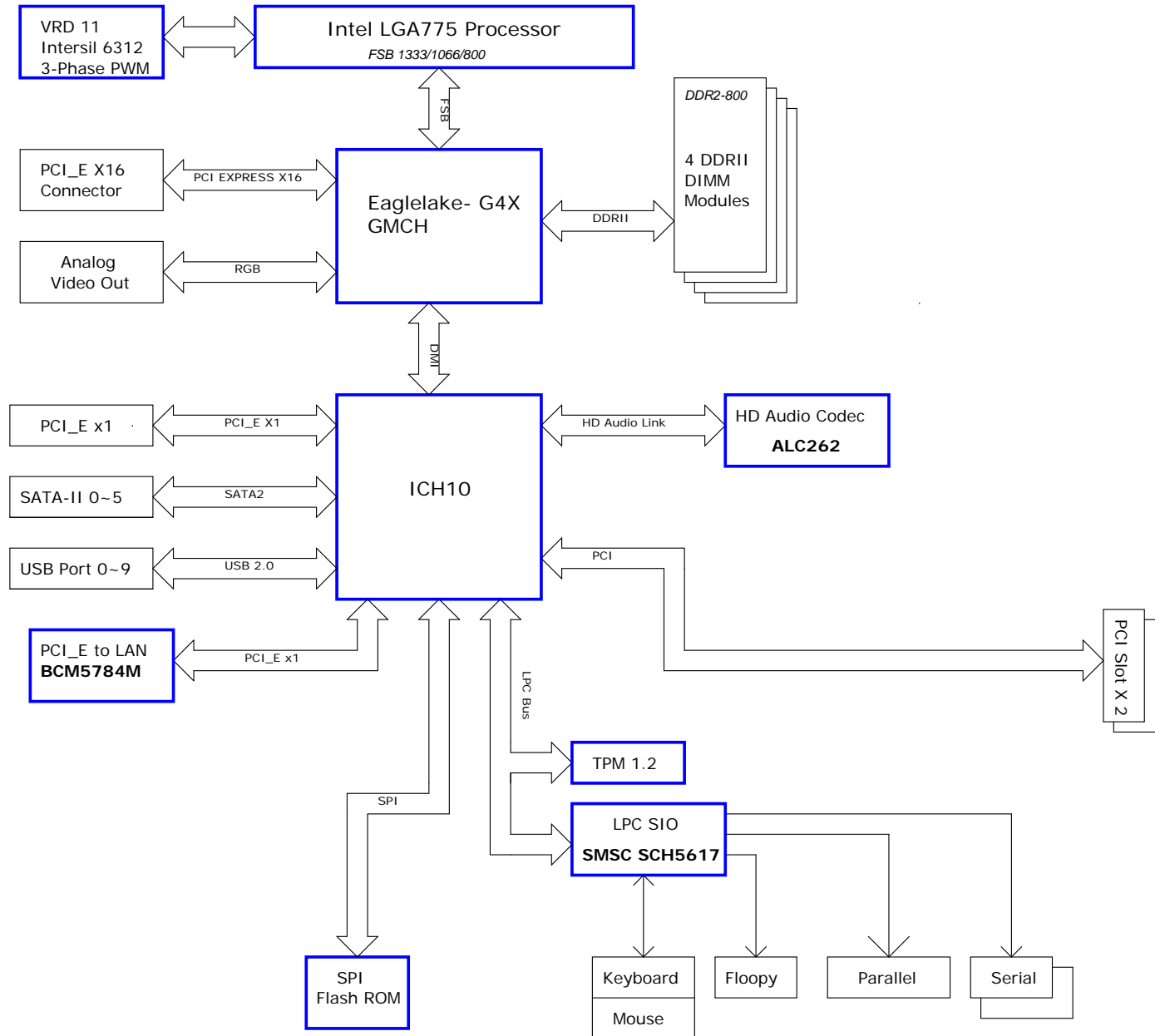
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Rev 0B

Date: Thursday, July 03, 2008

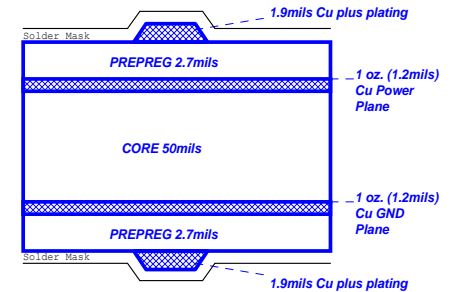
Sheet 1 of 35

Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/7.5/4.5/7.5/15
 SATA - 95ohm : 15/8/4/8/15
 LAN - 100ohm : 15/10/4/10/15
 PCIe - 95ohm : 15/8/4/8/15

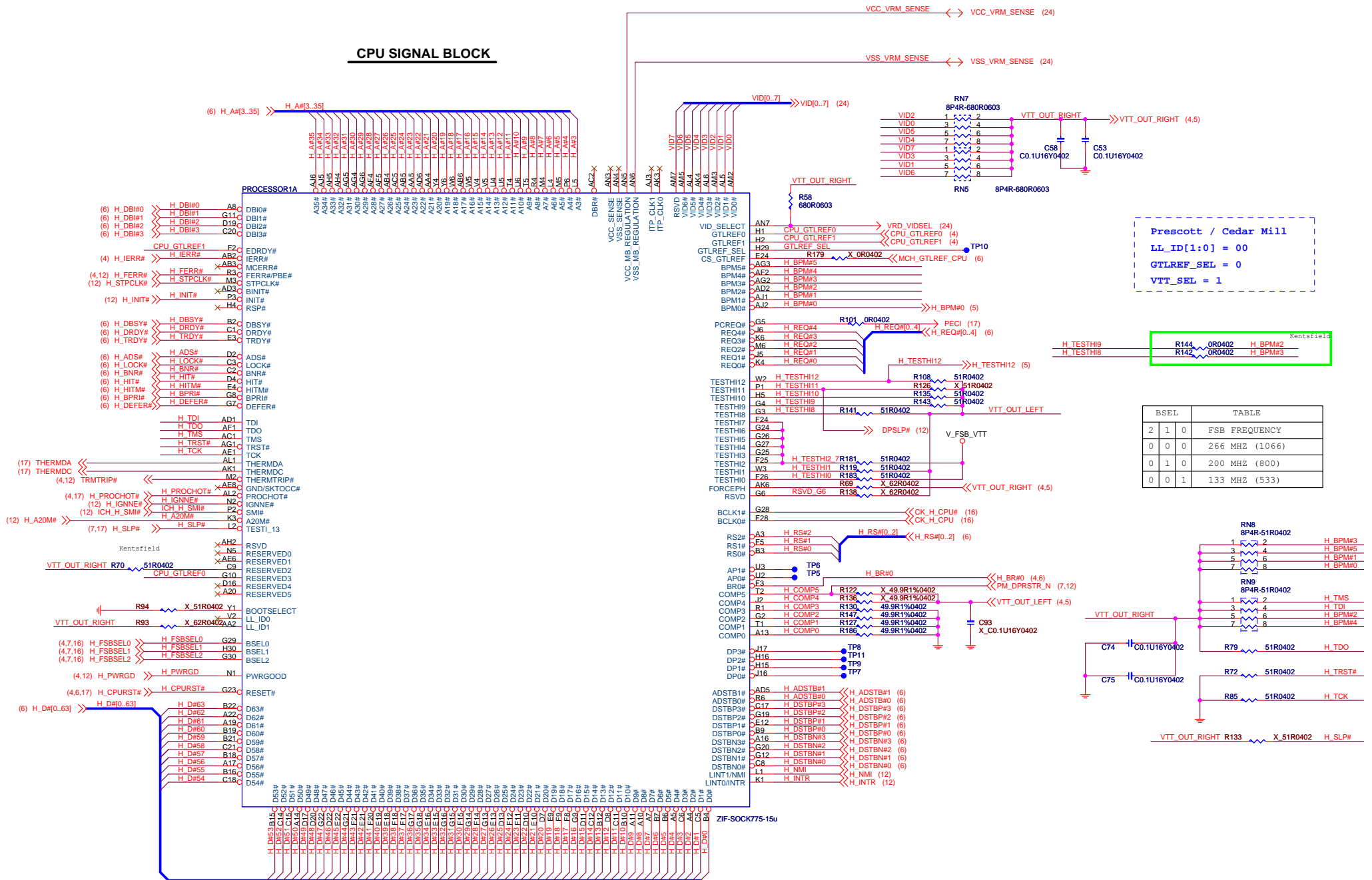


MICRO-STAR INT'L CO.,LTD

MS-7428N1

Size	Document Description	Rev
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Date: Thursday, July 03, 2008	Sheet 2 of 35	

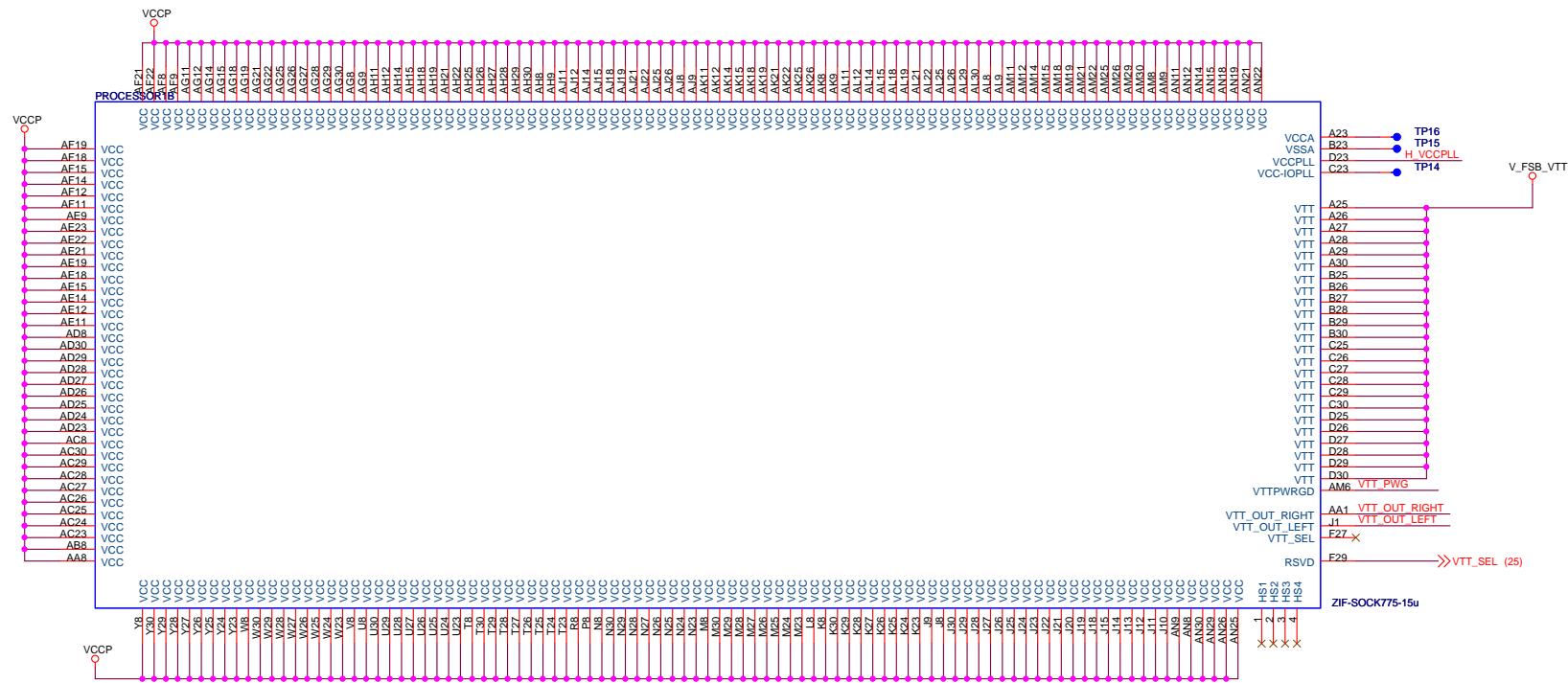
CPU SIGNAL BLOCK



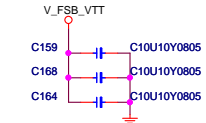
MICRO-STAR INT'L CO.,LTD

MS-7428N1

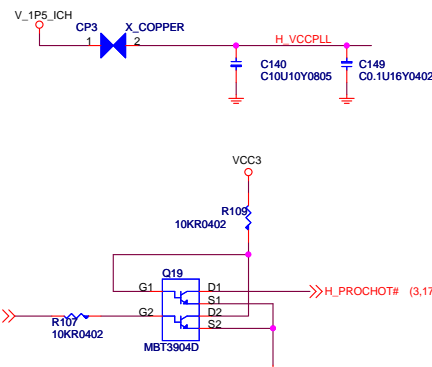
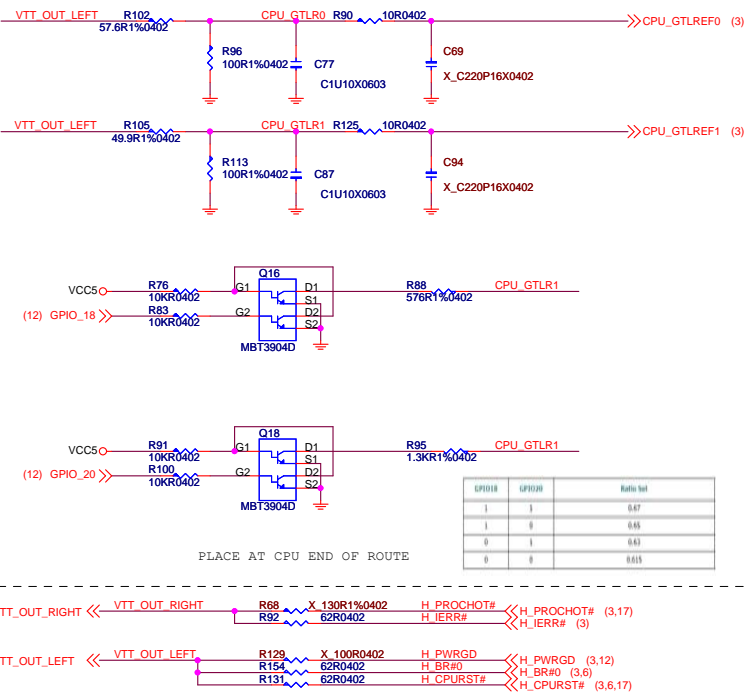
Size Custom	Document Description Intel LGA775 - Signals	Rev 0B
Date: Thursday, July 03, 2008		Sheet 3 of 35



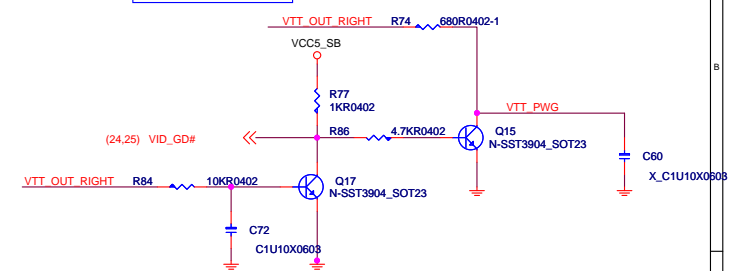
BIOS writers Guide
PDG:page109



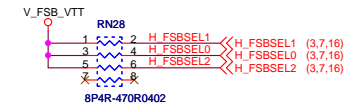
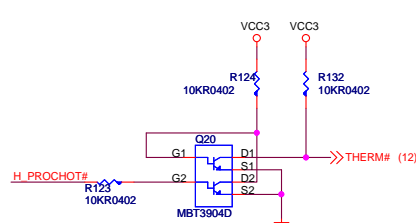
CAPS FOR FSB GENERIC



VTT_PG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns



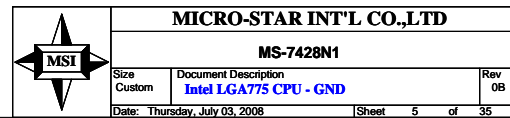
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED

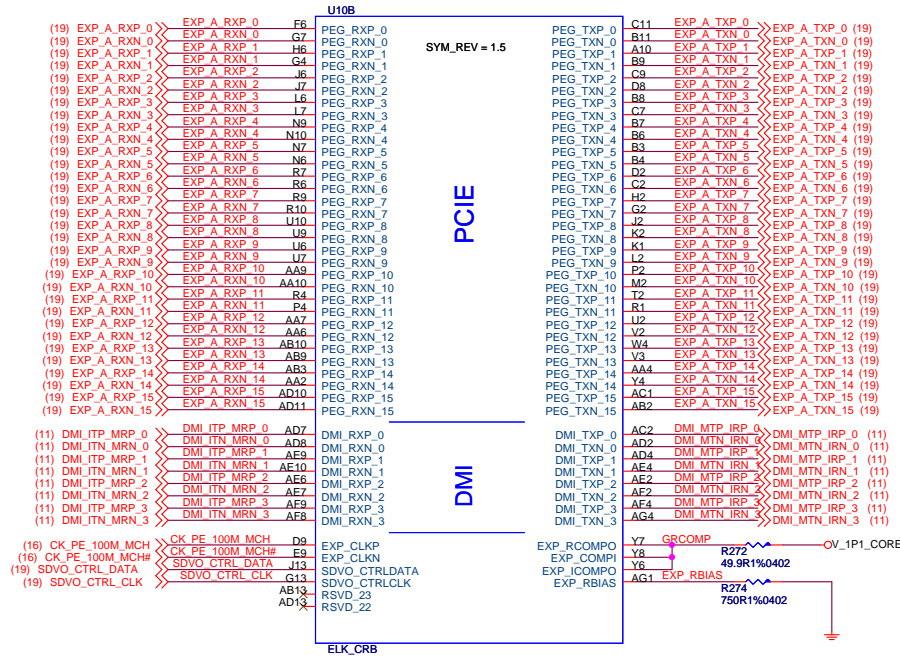
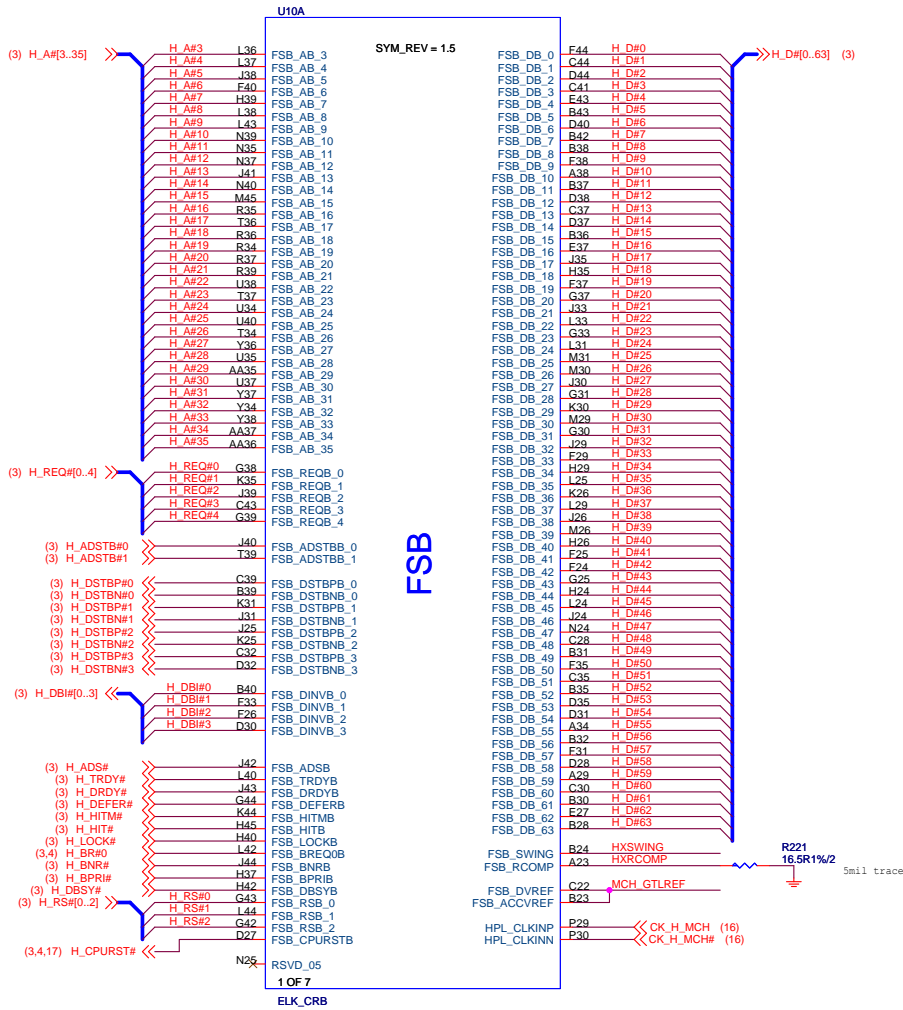


PLACE AT ICH END OF ROUTE

MSI

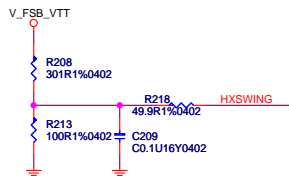
MICRO-STAR INT'L CO.,LTD		
MS-7428N1		
Size	Document Description	Rev
Custom	Intel LGA775 - Power	0B
Date: Thursday, July 03, 2008	Sheet 4 of 35	





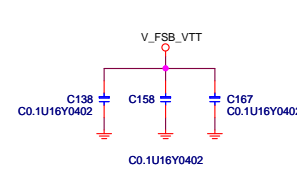
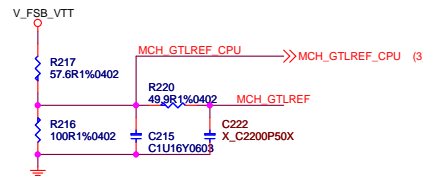
HD_SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD_SWING S/B 1/4*VTT +/- 2%

PLACE DIVIDER RESISTOR NEAR VTT



GTLREF VOLTAGE SHOULD BE 0.635*VTT=0.7V

100 OHM OVER 200 RESISTORS



MSI

MICRO-STAR INT'L CO.,LTD

MS-7428N1

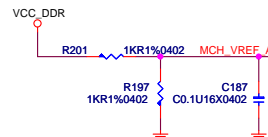
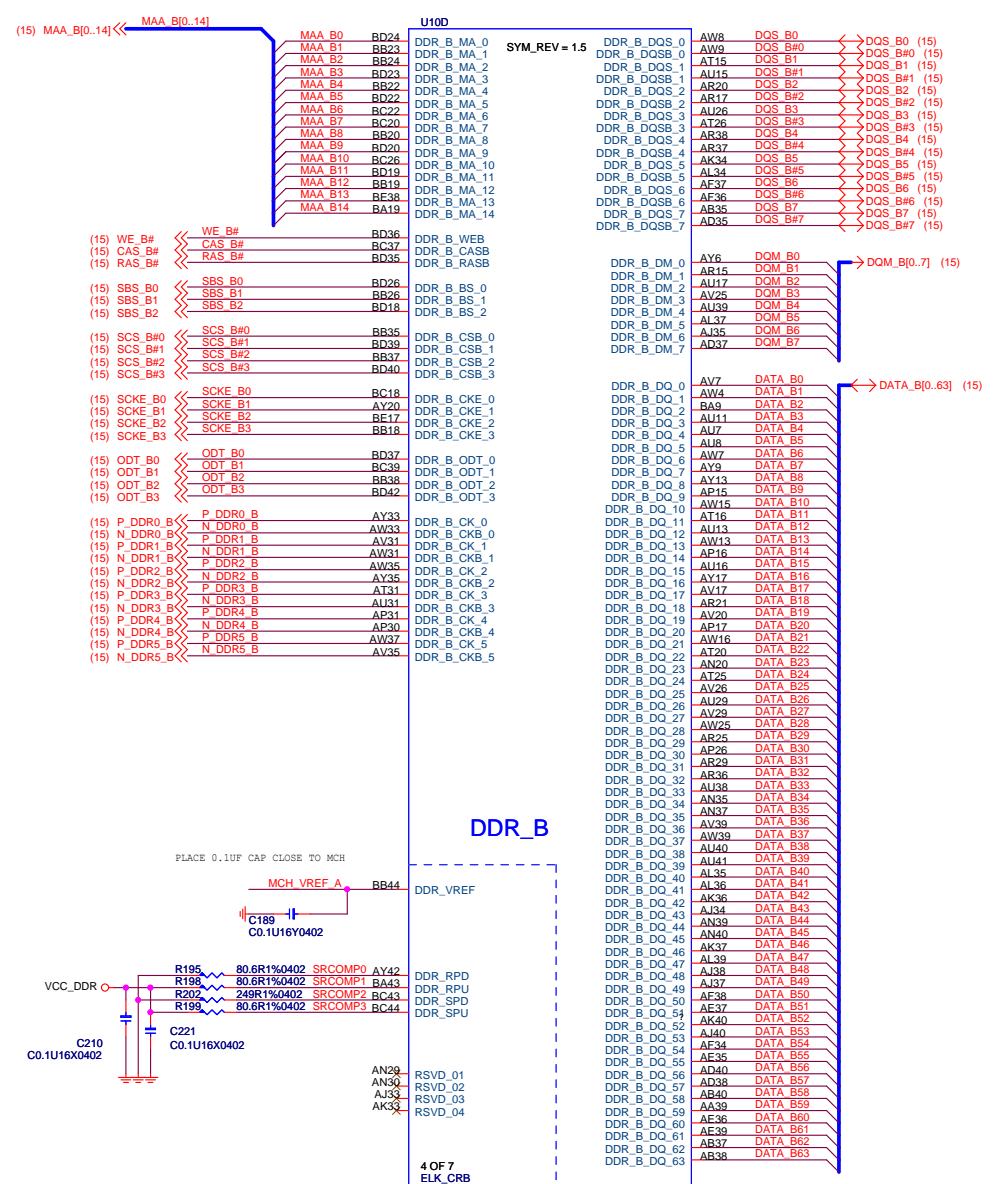
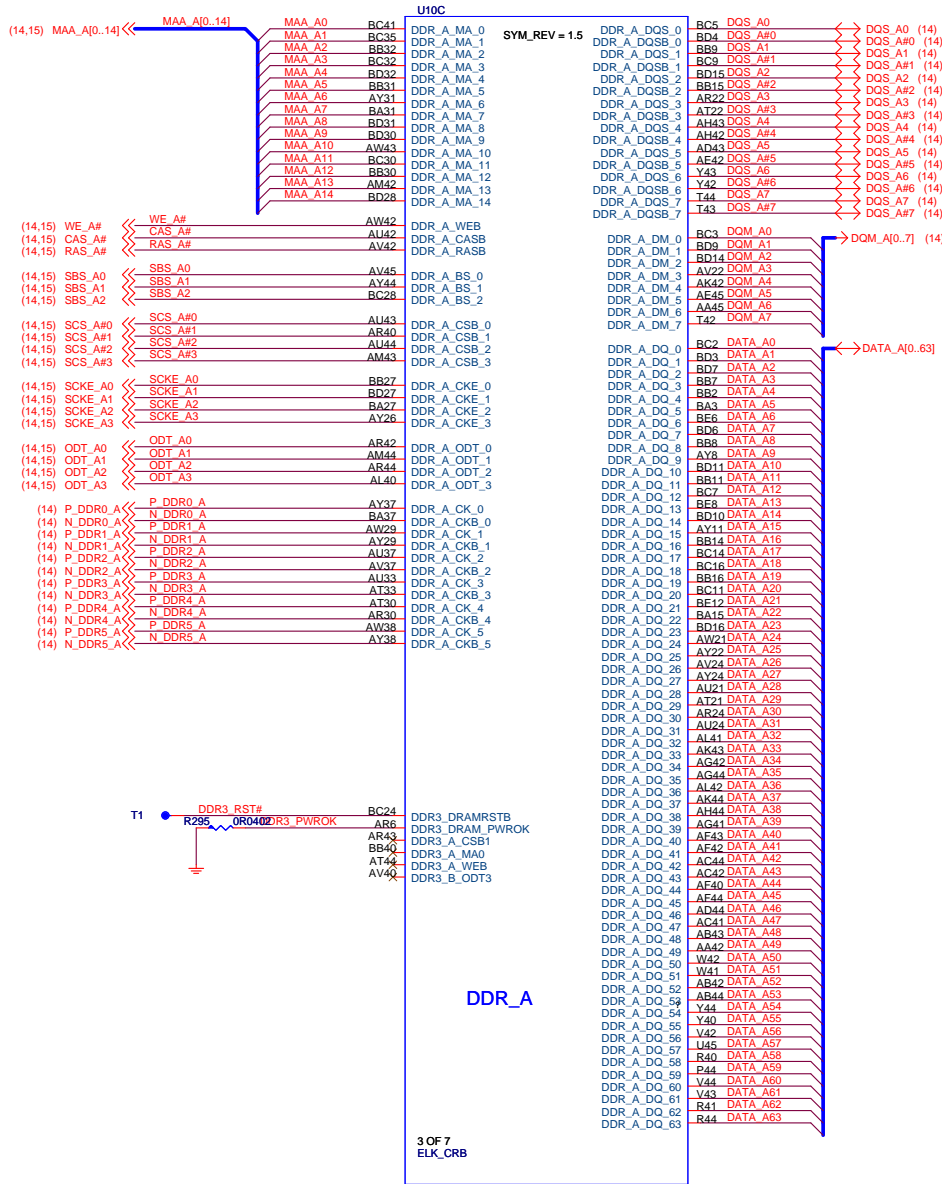
Size Custom

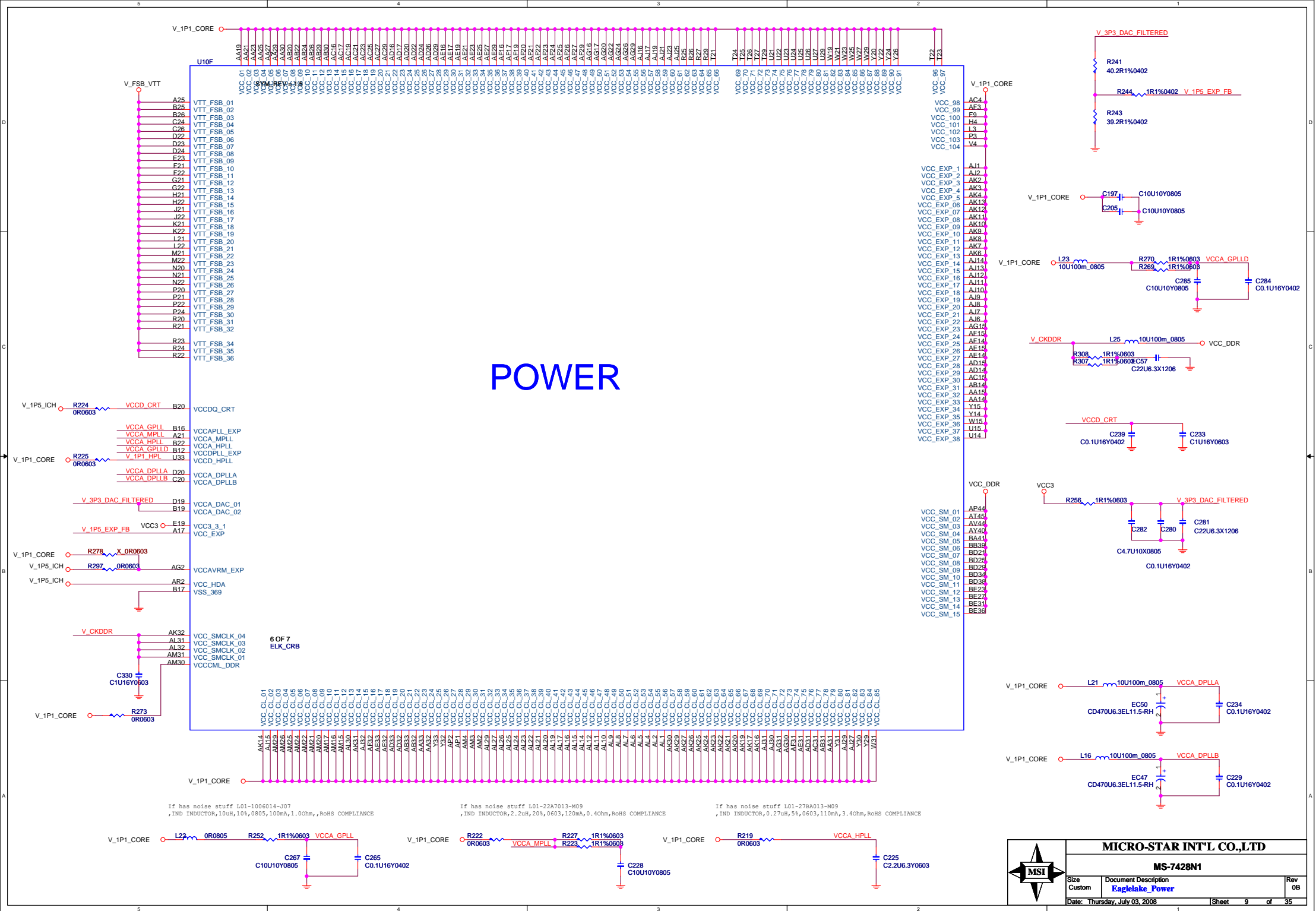
Document Description Eaglelake FSB/PCIE

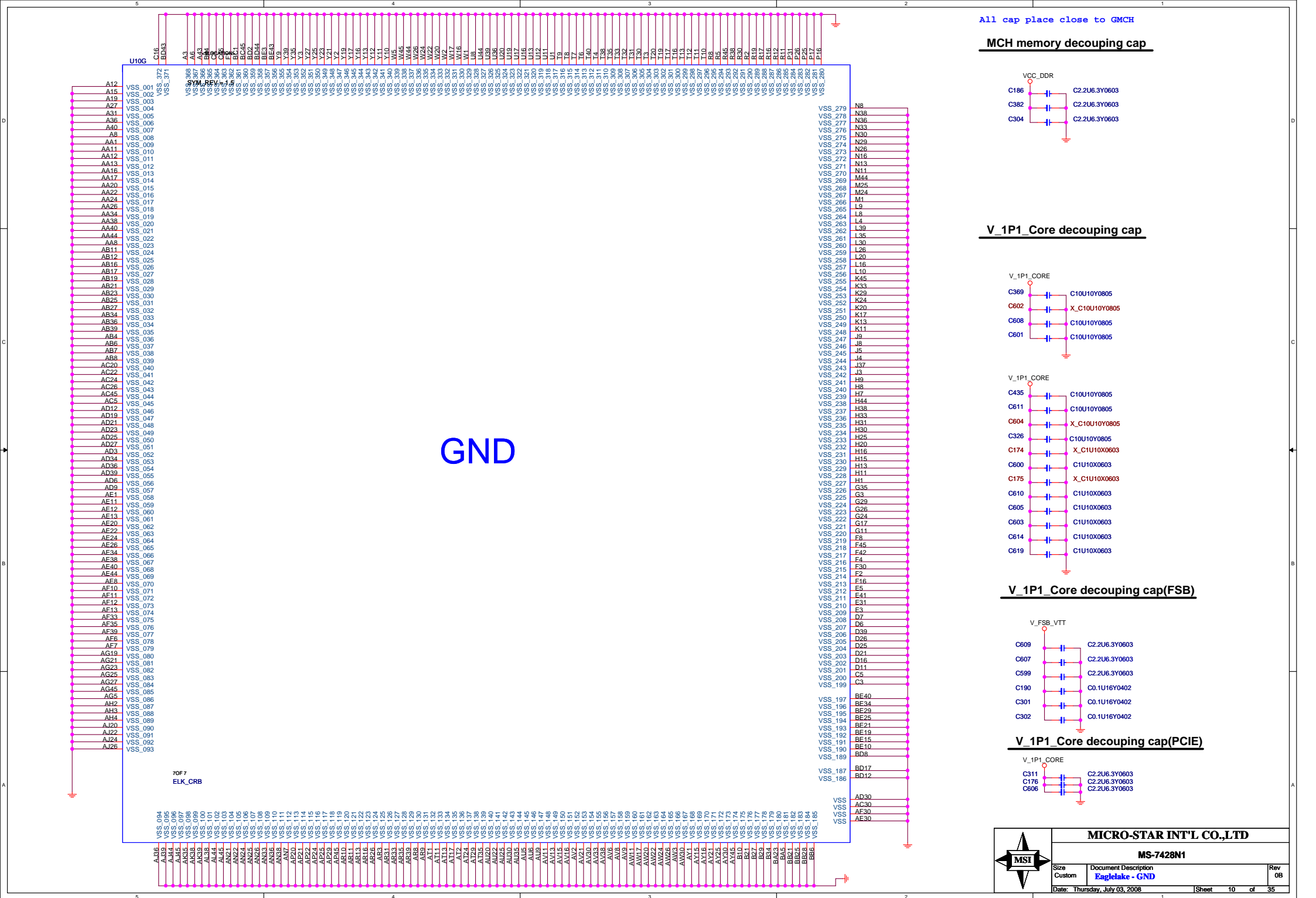
Rev 0B

Date: Thursday, July 03, 2008

Sheet 6 of 35

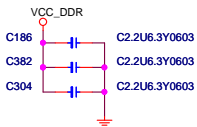




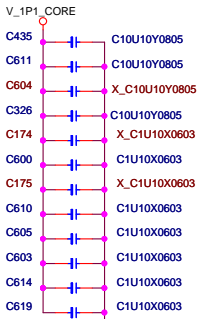
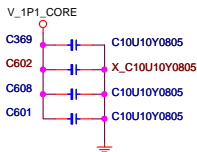


All cap place close to GMCH

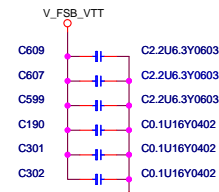
MCH memory decouping cap



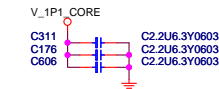
V_1P1_Core decouping cap



V_1P1_Core decouping cap(FSB)



V_1P1_Core decouping cap(PCIE)

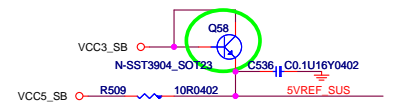
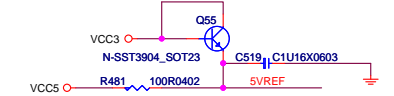
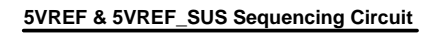


MICRO-STAR INT'L CO.,LTD

MS-7428N1

Size Custom	Document Description Eaglelake - GND	Rev 0B
Date: Thursday, July 03, 2008	Sheet 10 of 35	

HDMI	VccHDA	VccSusHDA	Description
Enable	1.5V	1.5V_SB	STAFF R485 R499 (R499=0 ohm)
Disable (Default)	3.3V	VCC3_SB	STAFF R484 R499 R568 (R499=18 ohm, R568=15ohm)



MS-7428N1

	Document Description
	ICH10 - Power_GND

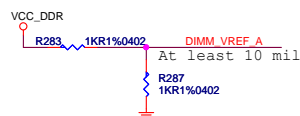
Rev
0B

Date: Thursday, July 03, 2008	Sheet 13 of 35
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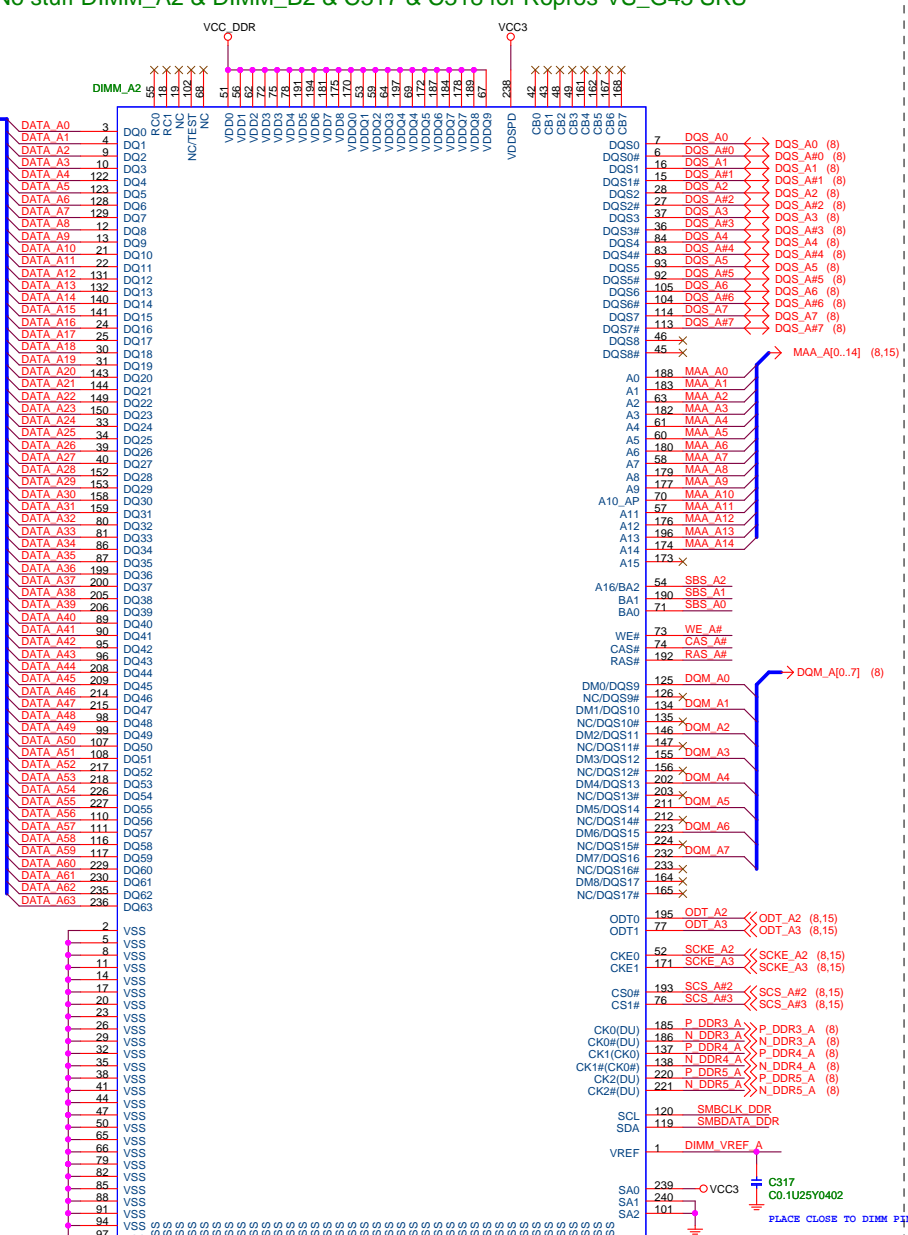
No stuff DIMM_A2 & DIMM_B2 & C317 & C318 for Ropros-VS_G43 SKU



DDRII DIMM_A1



ADDRESS: 000
0xA0



DDRII DIMM_A2

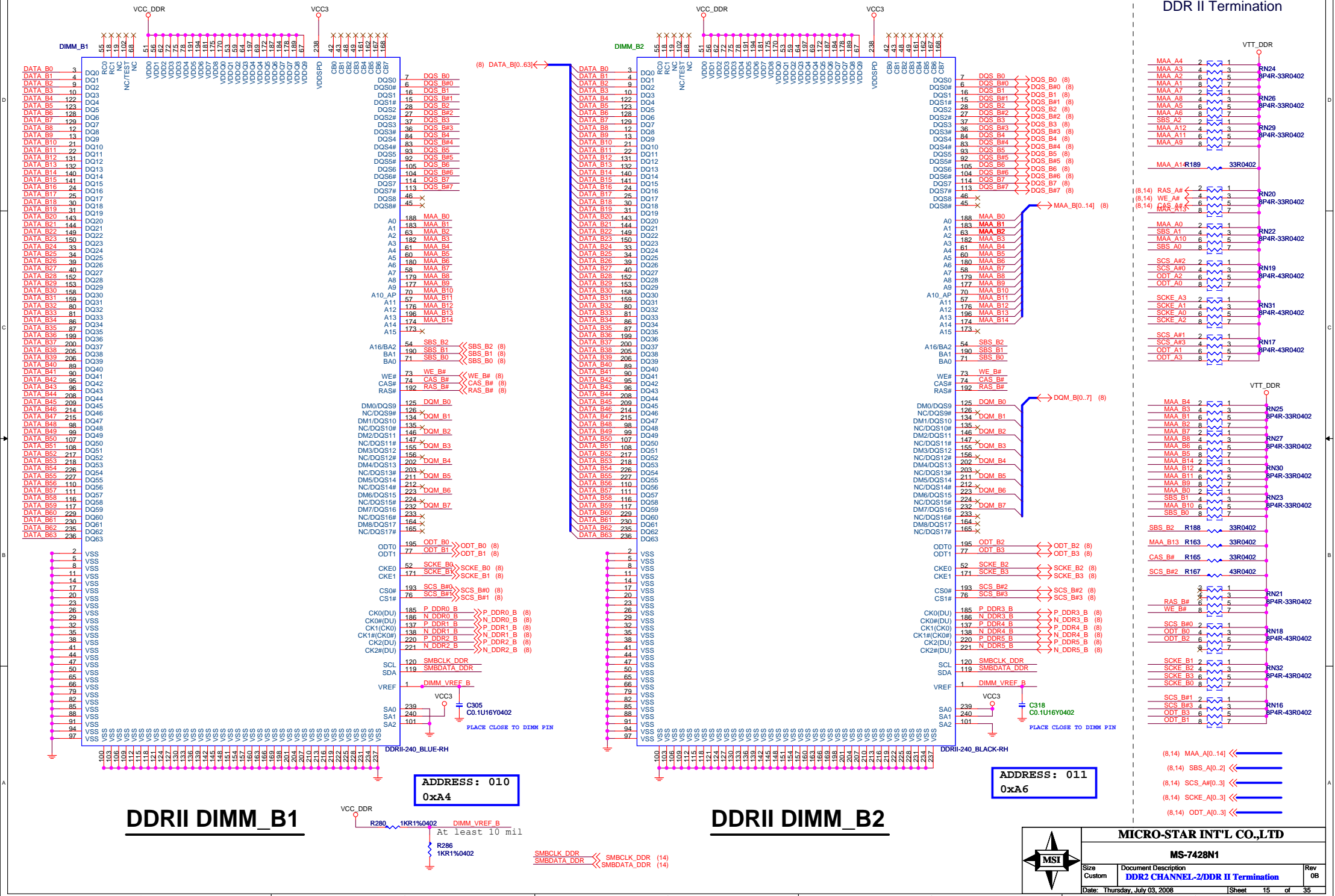
ADDRESS: 001
0xA2



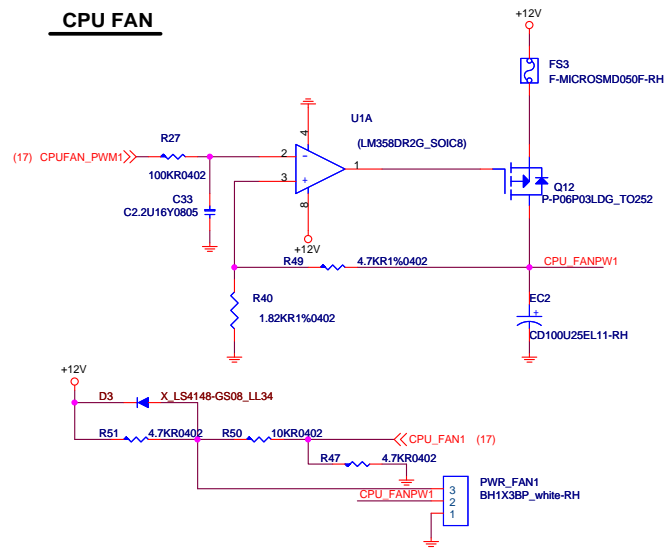
MICRO-STAR INT'L CO.,LTD

MS-7428N1

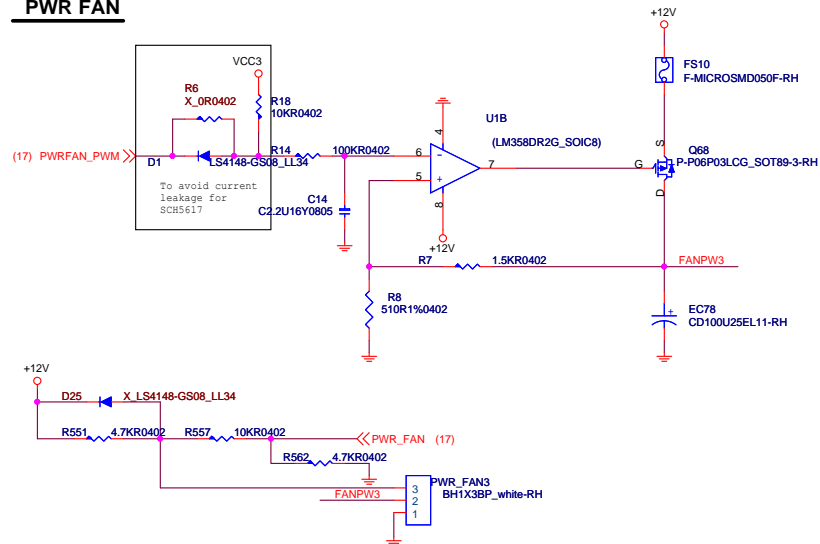
Size	Document Description	Rev
Custom	DDR2 CHANNEL-1	0B
Date: Thursday, July 03, 2008	Sheet 14 of 35	



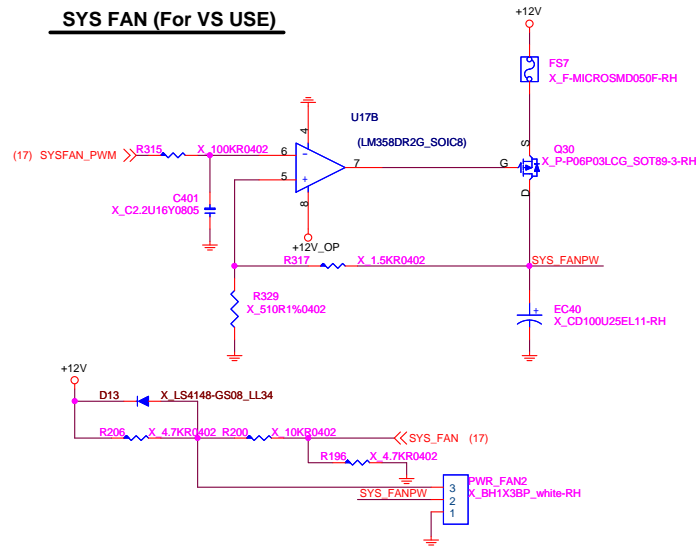
CPU FAN



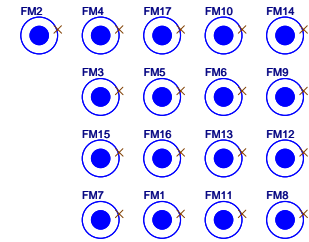
PWR FAN



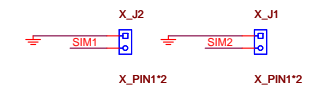
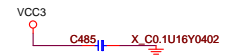
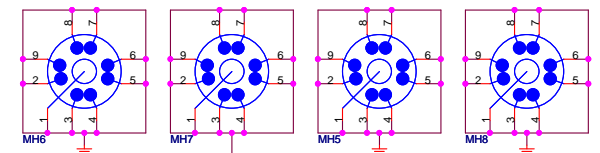
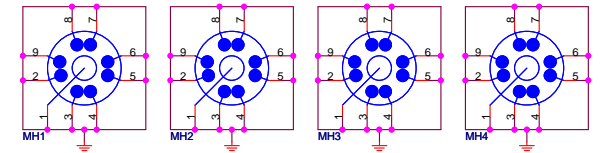
SYS FAN (For VS USE)



Optical Fiducial Marks



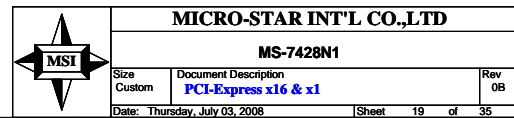
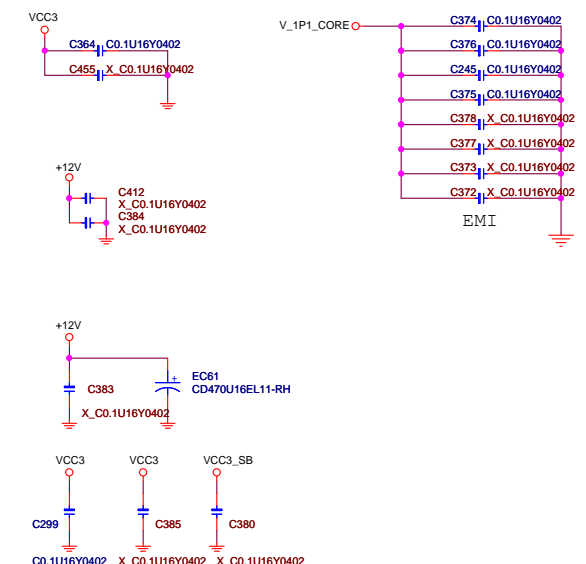
Mounting Holes



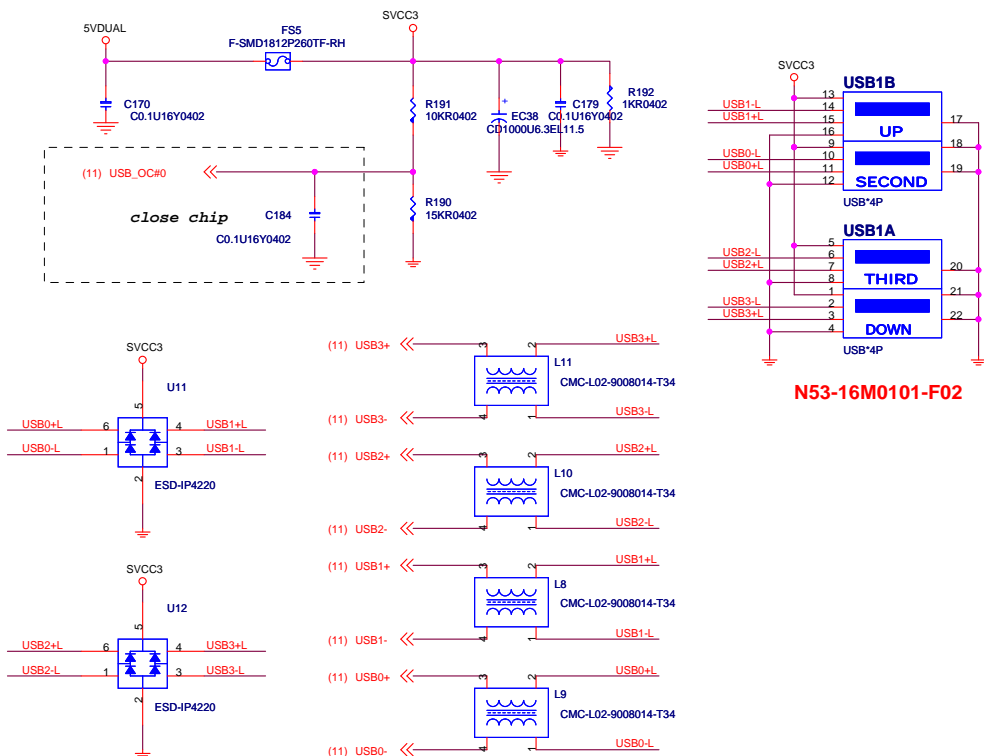
	MICRO-STAR INT'L CO.,LTD		
	MS-7428N1		
	Size	Document Description	Rev
	Custom	CPU/SYS/PWR FAN	0B
Date: Thursday, July 03, 2008		Sheet 18 of 35	

PEG_PINB7 R309 0R0402

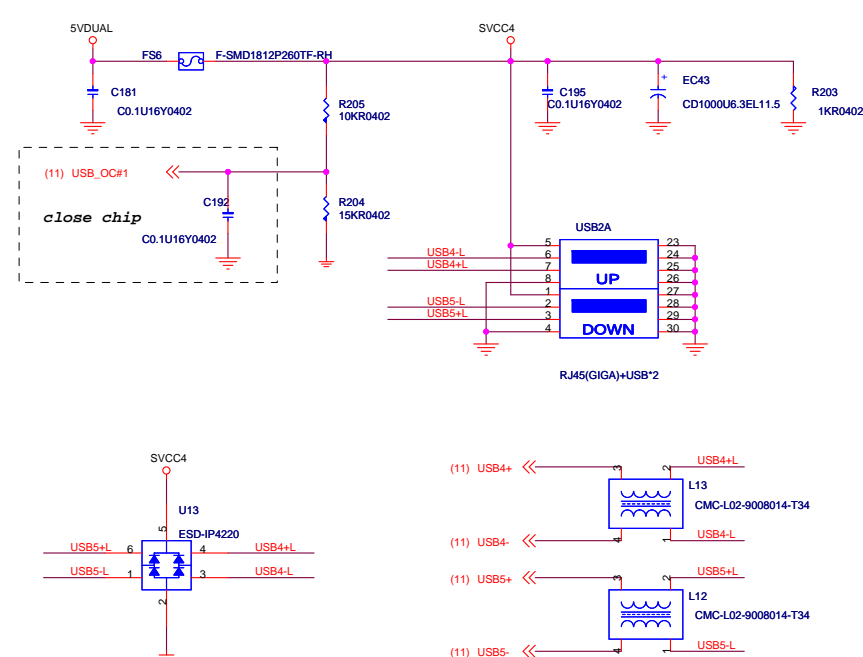
PCI EXPRESS 16-PORT



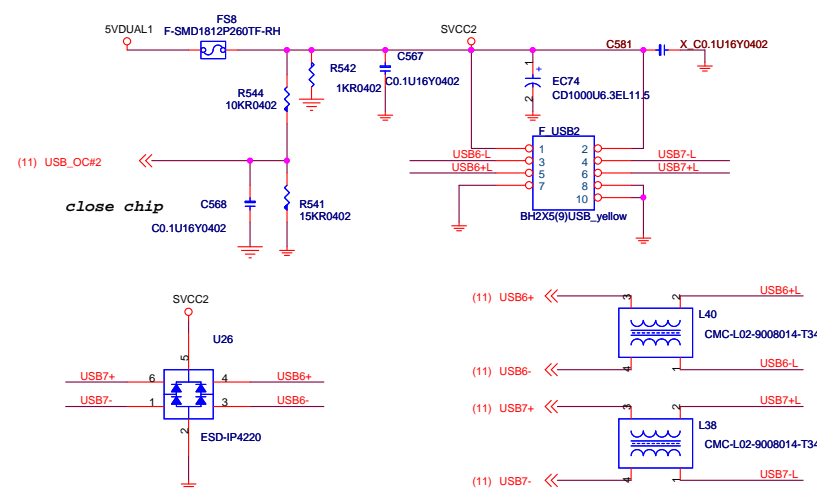
REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3 Iout=2A



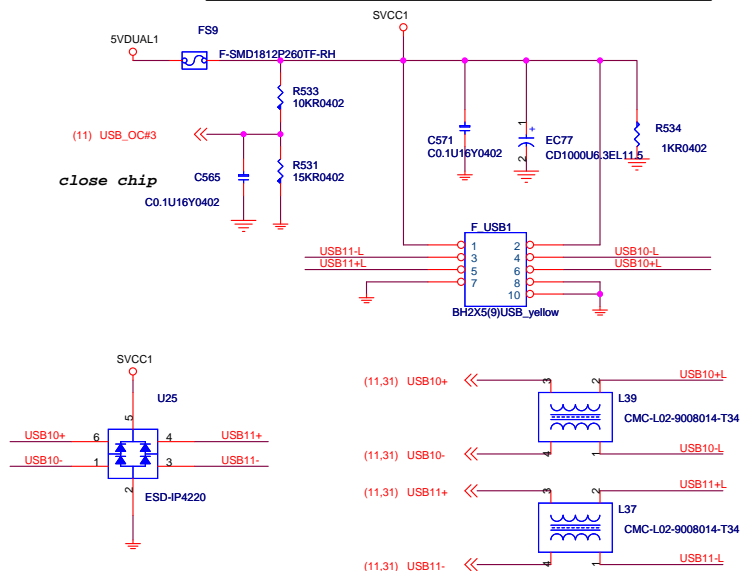
REAR PANEL USB CONNECTOR FOR USB PORT 4,5 Iout=1A



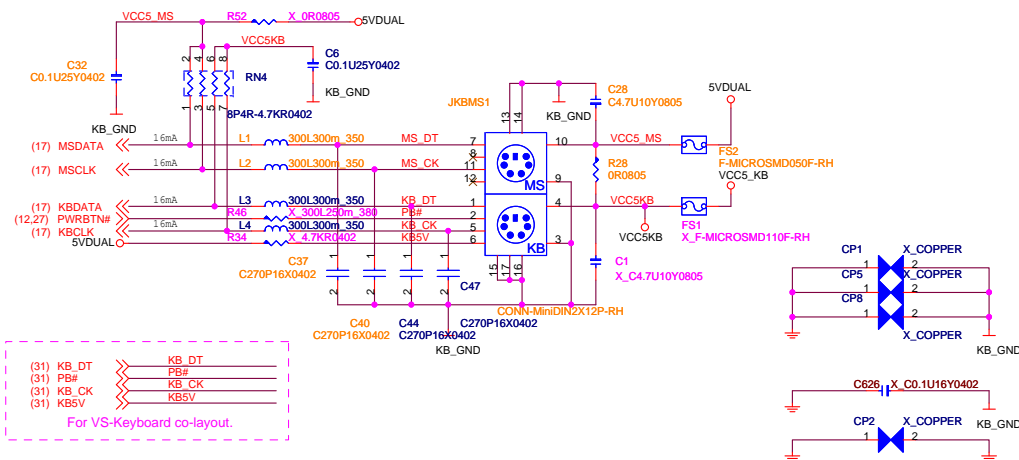
Memory card reader USB CONNECTOR FOR USB PORT 8,9 (pinth 2.0) Iout=1A



Front USB PORT 10,11 (right angel type) Iout=1A

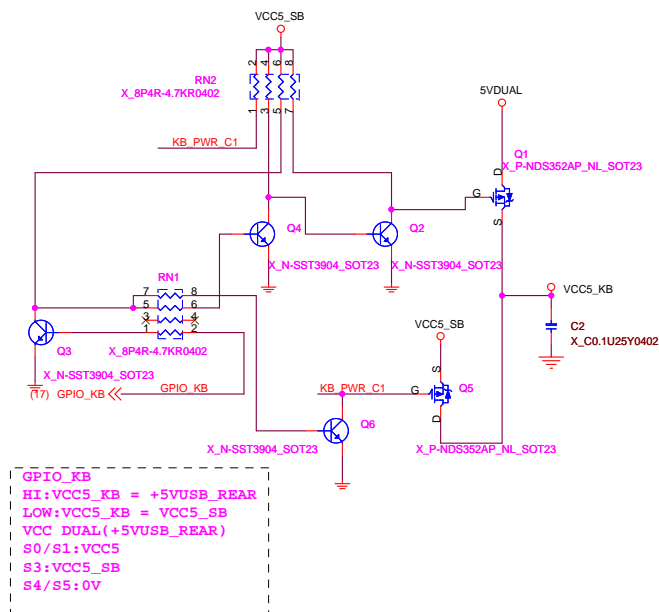


PS2 KEYBOARD & MOUSE CONNECTOR

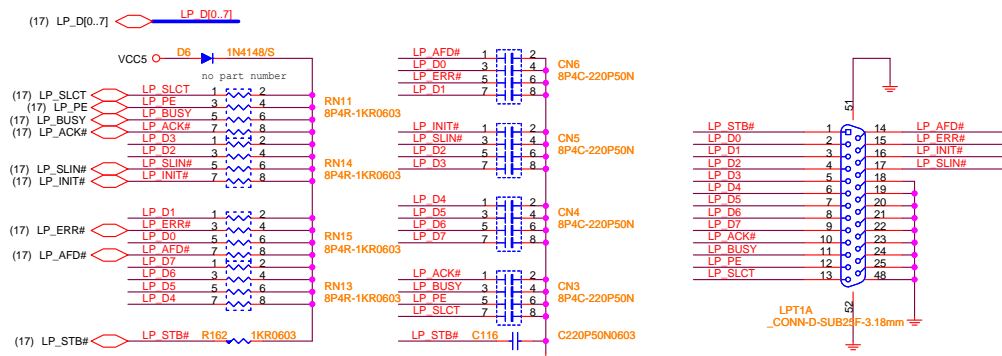


	FS2	R20	C24	L1	L2	C33	C33	C34	C38	FS1	C1	R27	R36
ROPROS-MA	V	V	V	V	V	V	V	V	V	X	X	X	X
ROPROS-VS	X	X	X	X	X	X	X	X	X	V	V	V	V
ROPROS-NECCA	V	V	V	V	V	V	V	V	V	X	X	X	X

K/B Power supply function for ROPROS-VS



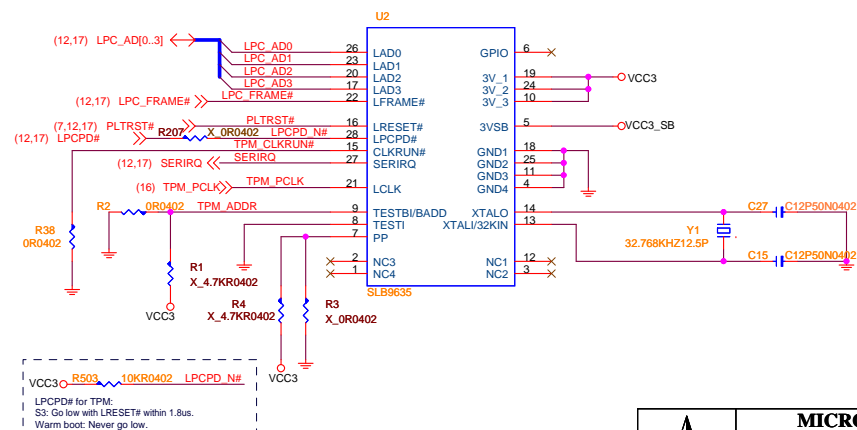
PARALLAL PORT



T.P.M FOR ROPROS-MA

TPM 1.2

IO Address:0x02E



MICRO-STAR INT'L CO.,LTD

MS-7428N1

Size	Document Description
100	100
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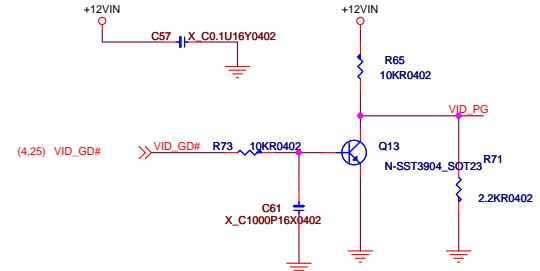
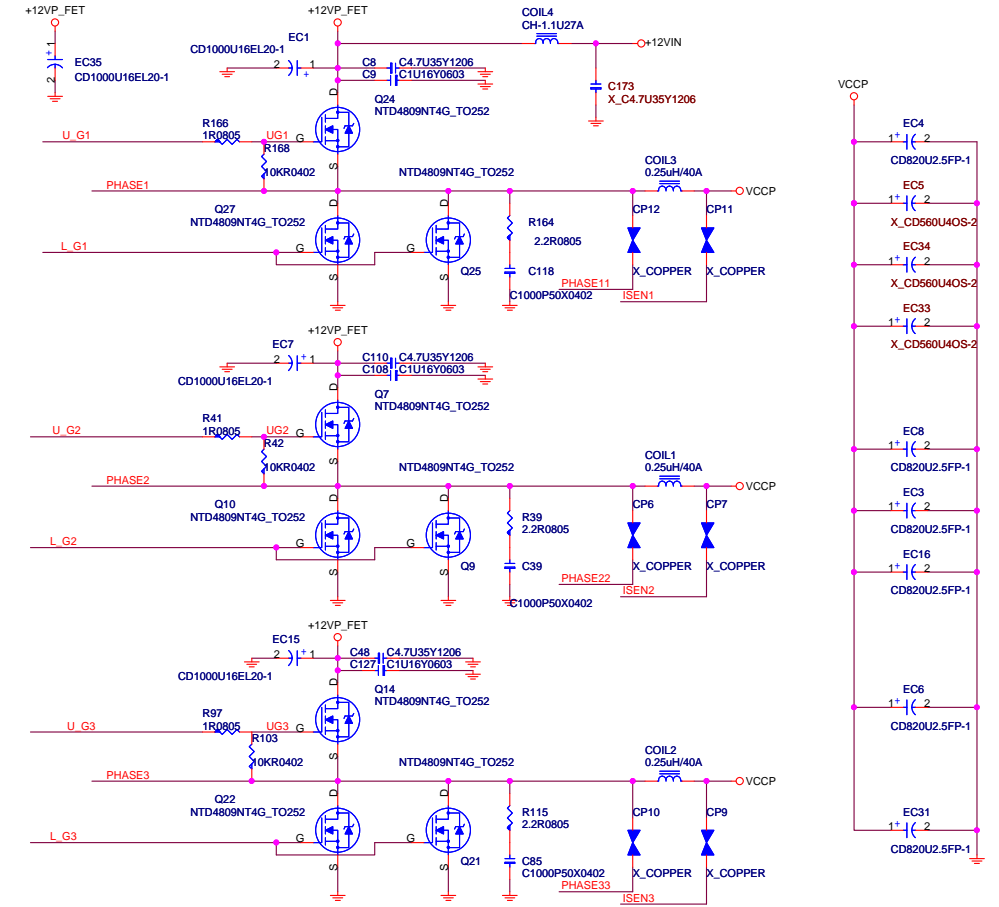
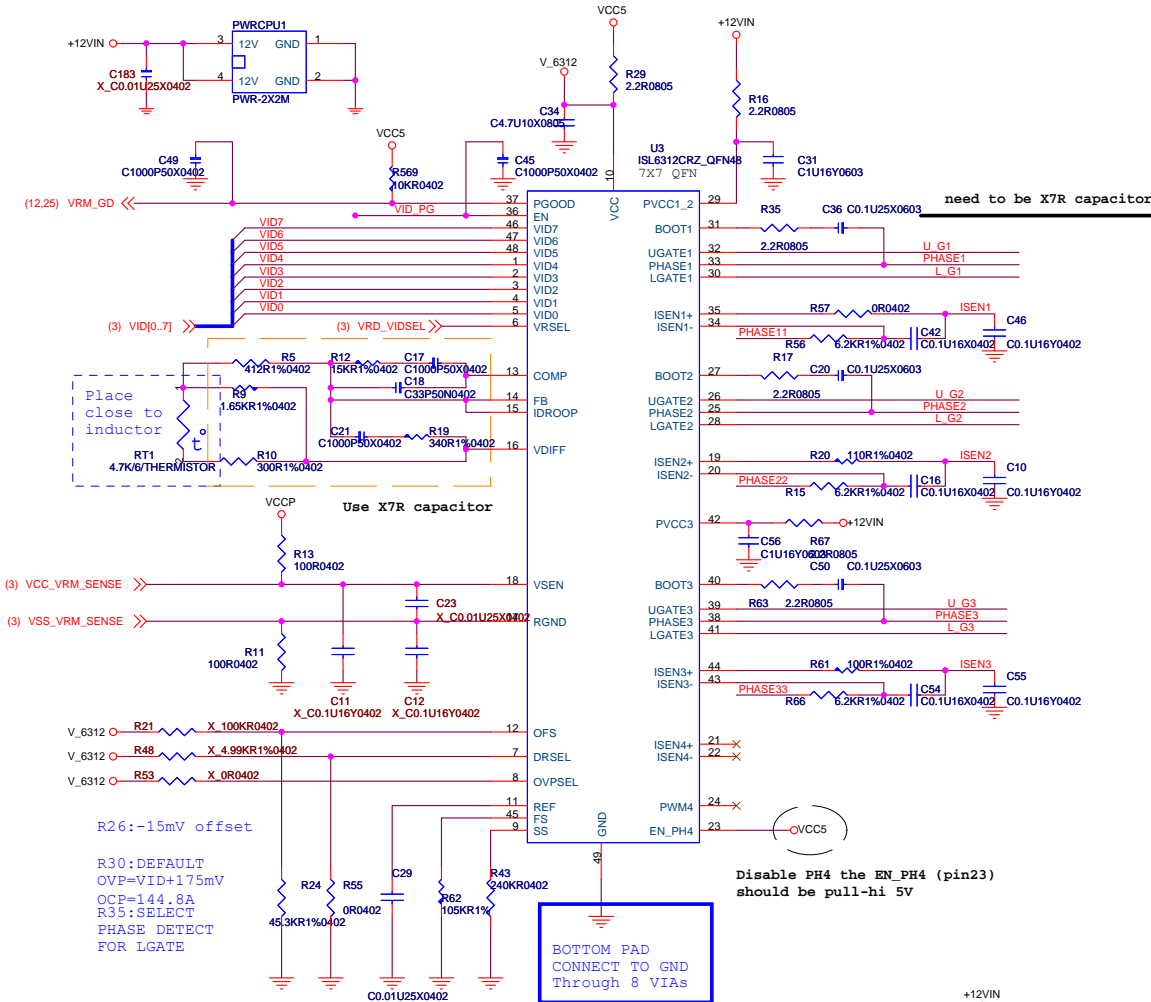
Custom	KB/MS/TPM/PARALLEL
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Rev

Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
C100U2SP
CD560U40S-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

mosfet/n-channel, P0903BDG, SMT/TO252, Rds(on)=9.5mΩ(10V/25A), Vgs(on)=1~3V, Id=50A, Ciss=1800pf, Qg=50nC, Vds=25V, Vgs=±20V, RoHS compliance
mosfet/n-channel, P75N02LDG, SMT/TO252, Rds(on)=7mΩ(10V/30A), Vgs(on)=1~3V, Id=75A, Ciss=5000pf, Qg=140nC, Vds=25V, Vgs=±20V, RoHS compliance
ESR<13mΩ, Ripple cur.<2.7A, LC<12uA, 105C
CAP, OS-CON, 560u/4V, Dip-2/8*9/3.5mm, ESR<7mohm, Ripple cur.=6100mA, Lc. <500uA, SPEC series, RoHS compliance
ESR<12mΩ, Ripple cur.<2350mA, 105C, longlife change from 2000hrs to 3000hrs, KZJ series
, IND CHOKE, 0.25uH, 20%, DIP/8.5mm, 40A, 0.6mOhm, , , PEW, FERRITE, SQUARE, RoHS COMPLIANCE
IND CHOKE, 1.1uH, 20%, DIP/9mm, 25A, 1.4mOhm, 5.5T, 0.9mmx3, PEW, IRON, , LEAD FREE
CAP, EL, 1000u, 16V, Dip-8x20/3.5mm, 20%, 12mOhm, 2350mA, 105C, 3000hrs, RoHS COMPLIANCE



ACPI Controller MS-7

VDIMM LINEAR OR PWM SELECT

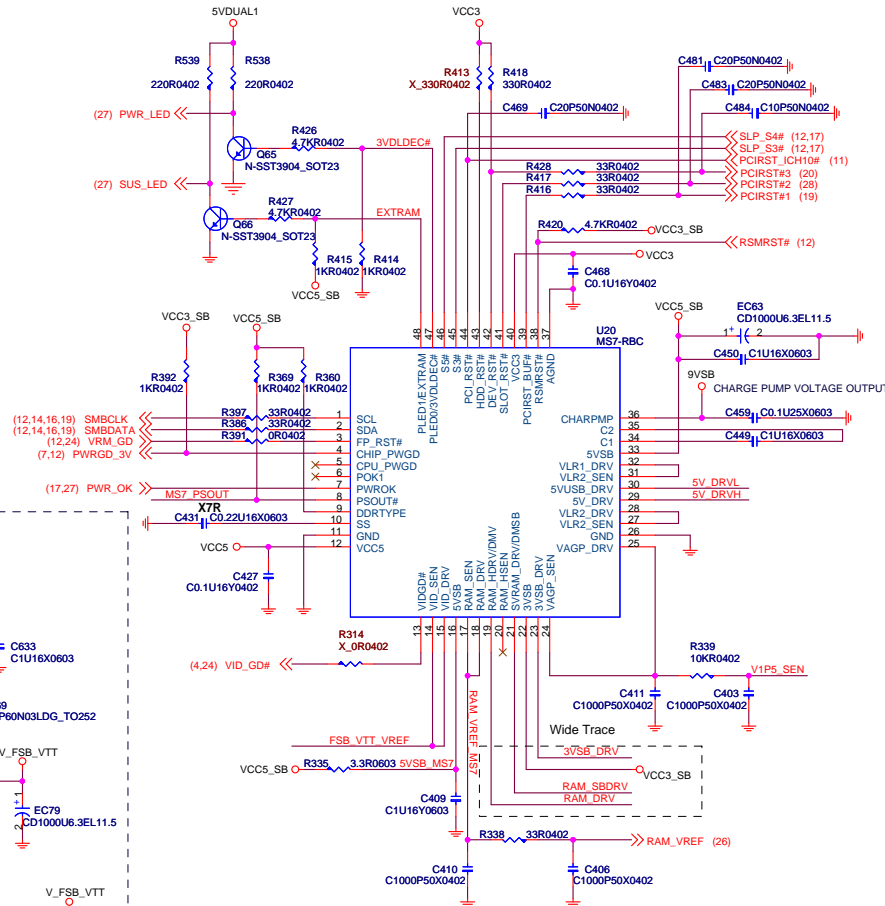
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

3VSB MODE SELECT

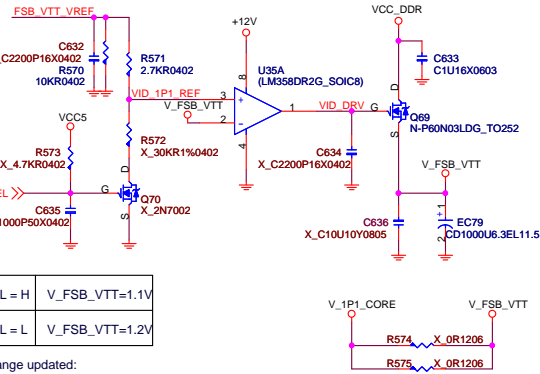
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

DDR AND DDR II VOLT SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

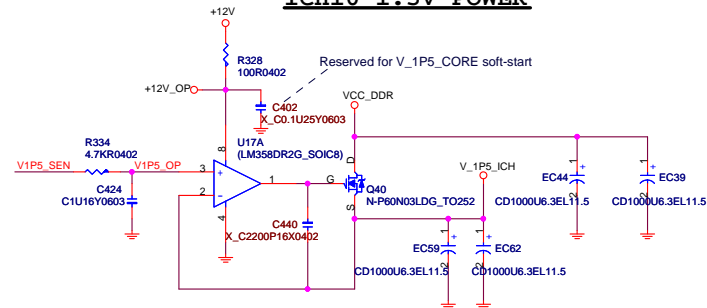


V_FSB_VTT POWER
(5.8A)

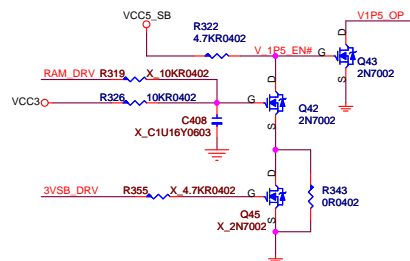


INTEL change updated:
FSB Vtt will change from 1.1V to 1.2V for All Intel® Series Express Chipsets and the 45nm Intel® Core™2 Quad and Intel® Core™2 Duo processors.

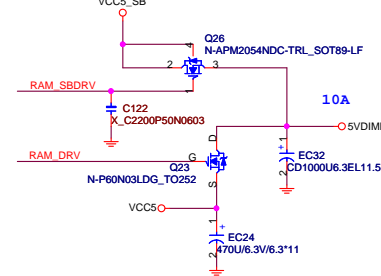
ICH10 1.5V POWER



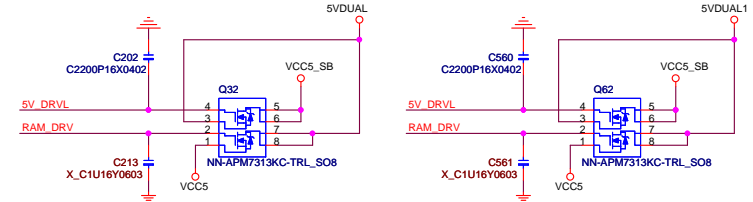
V1P5_SEN S3 power sequency



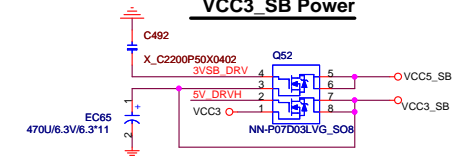
5V DIMM



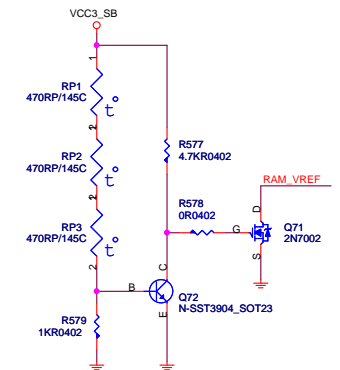
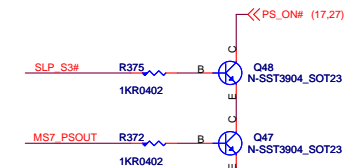
5V DUAL Power



VCC3_SB Power



PSON# & Posister for thermal sense



RP1/RP2/RP3: Place each posistor near PWM(Phase1&2) and Mem(PHASE_V_1P5)

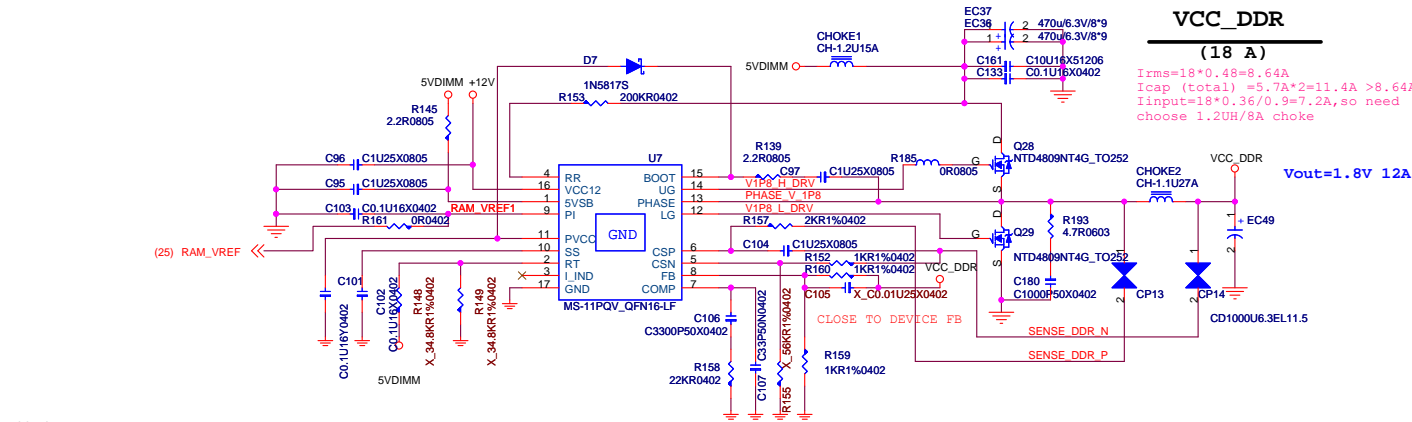
When temperature over 145 degree C,
the value of posistor will be multication.



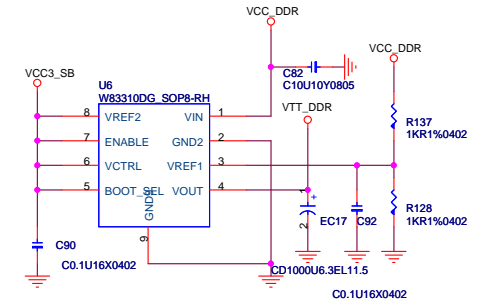
MICRO-STAR INT'L CO.,LTD

MS-7428N1

Size Custom	Document Description MS7 ACPI Controller	Rev 0B
Date: Thursday, July 03, 2008		Sheet 25 of 35

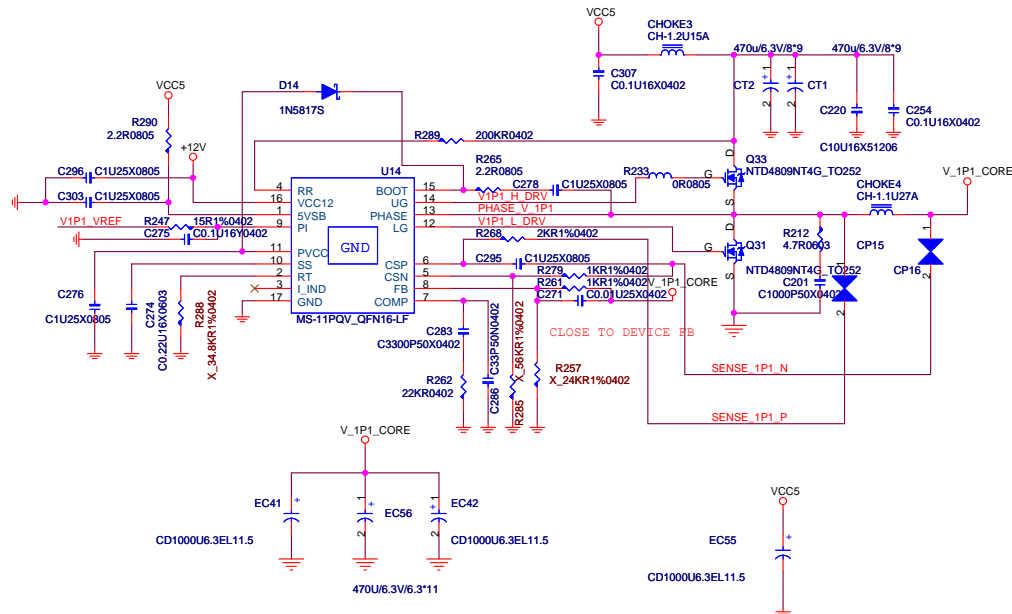


DDR VTT Power
(0.83A)

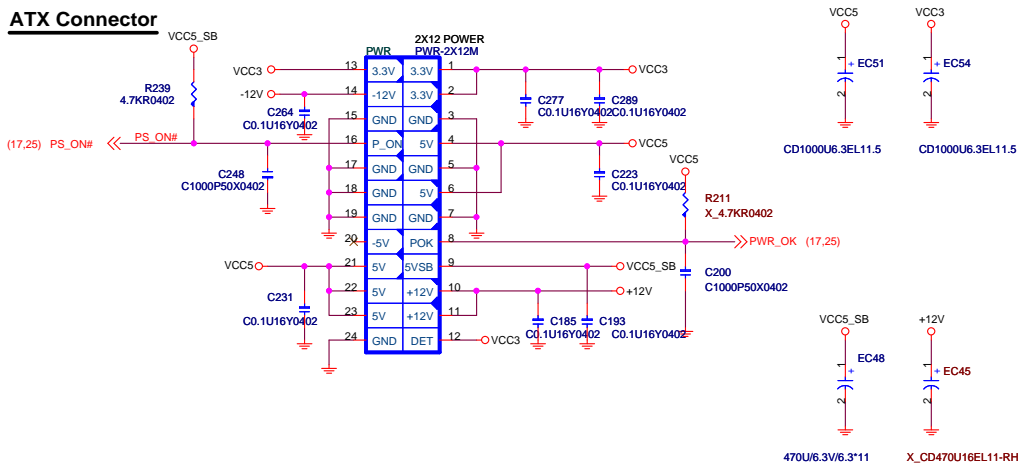


GMCH 1.1V POWER
(21.3A)

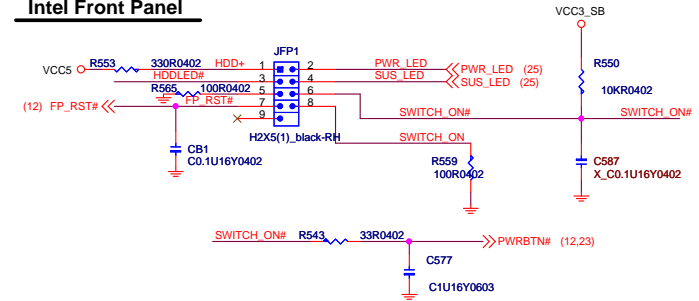
$I_{rms} = 21 \times 0.433 = 9.09A$
 $I_{cap} (total) = 5.7A \times 2 = 11.4A > 9A$
 $I_{input} = 21 \times 0.25 / 0.9 = 5.83A$, so need choose 1.2UH/8A choke



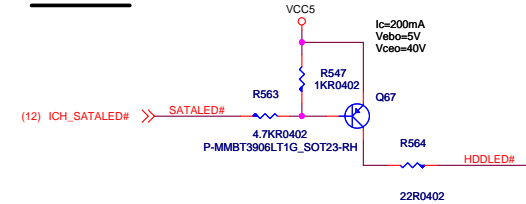
ATX Connector



Intel Front Panel

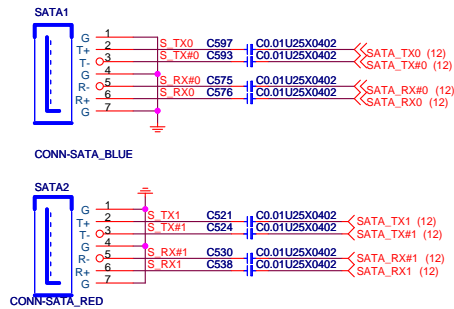


SATA LED

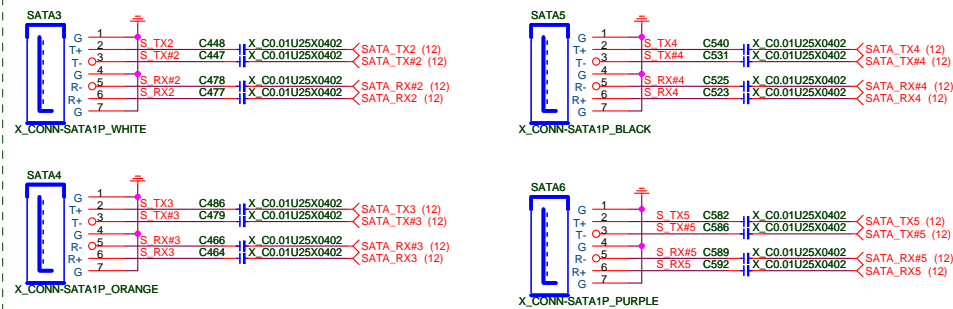


Serial ATA Connectors

SATA1&SATA2 for Ropros-E (MA/VS)



SATA3 to SATA6 for Poseidon-E

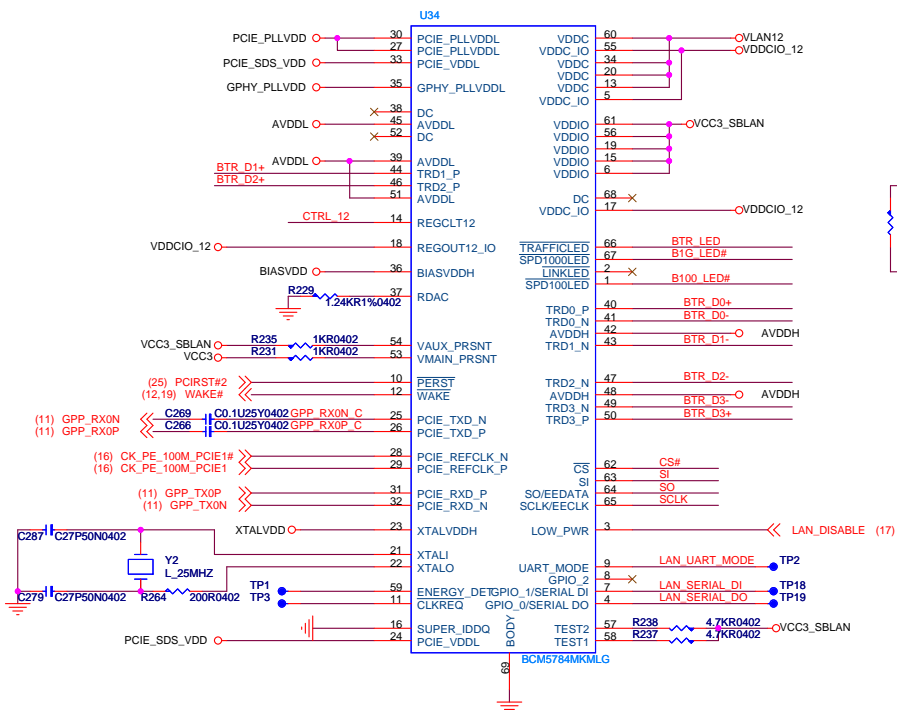


MICRO-STAR INT'L CO.,LTD

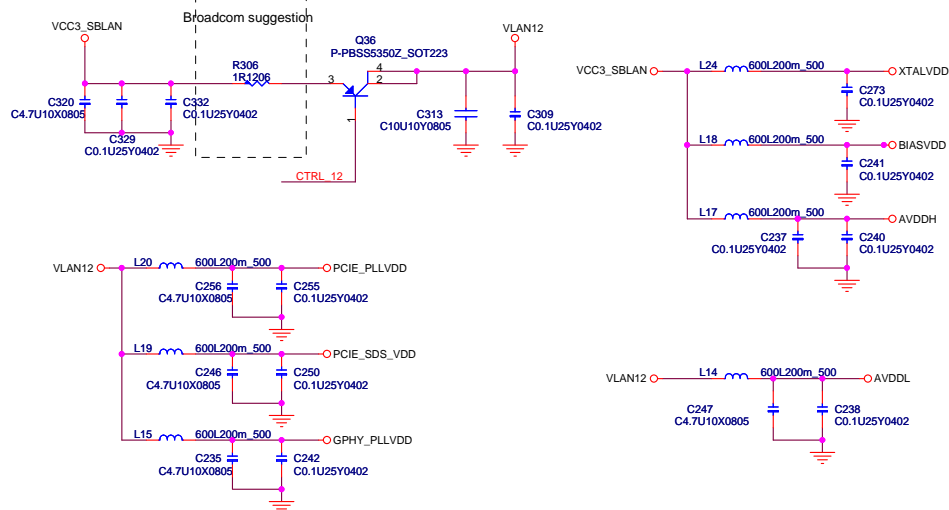
MS-7428N1

Size	Document Description	Rev
Custom	ATX, Front Panel, SATA Conn	0B
Date: Thursday, July 03, 2008	Sheet 27 of 35	

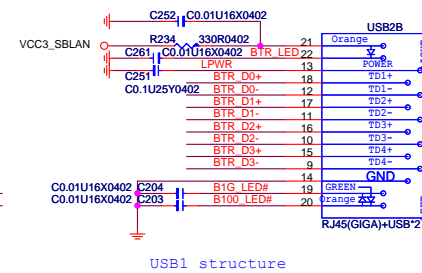
BCM5784M LAN CHIP (ROPROS-MA)



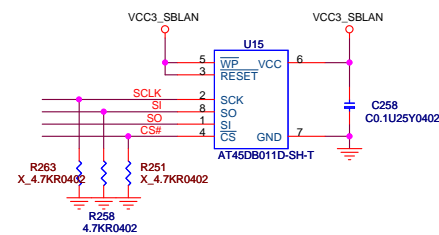
LAN 1.2 POWER



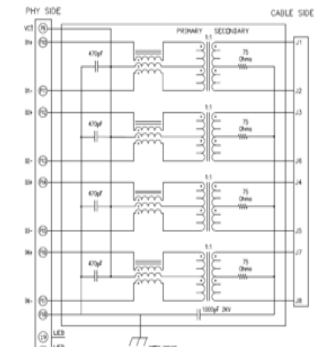
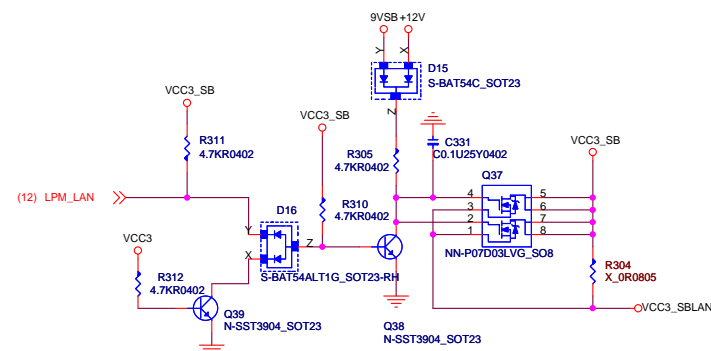
LAN Connector





LAN EEPROM

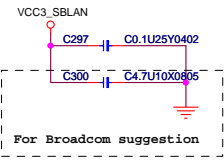
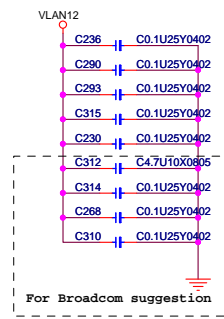
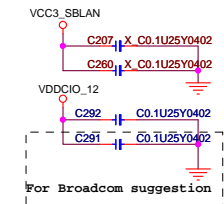


Power control for power consumption



Giga-Lan	
N58-22F0571-F02	
Link	Orange
Active	Blinking
1000	Orange
100	Green
10	None
21	
22	Orange
20	Green
19	 Orange

Bypass CAPs

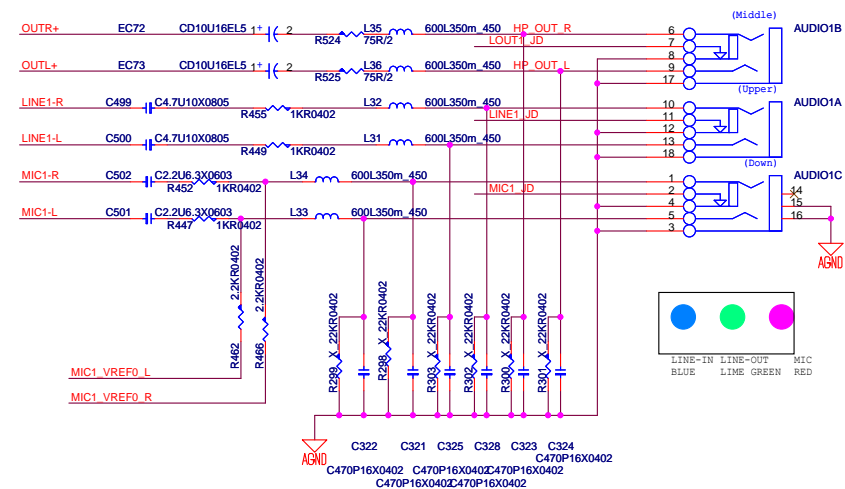
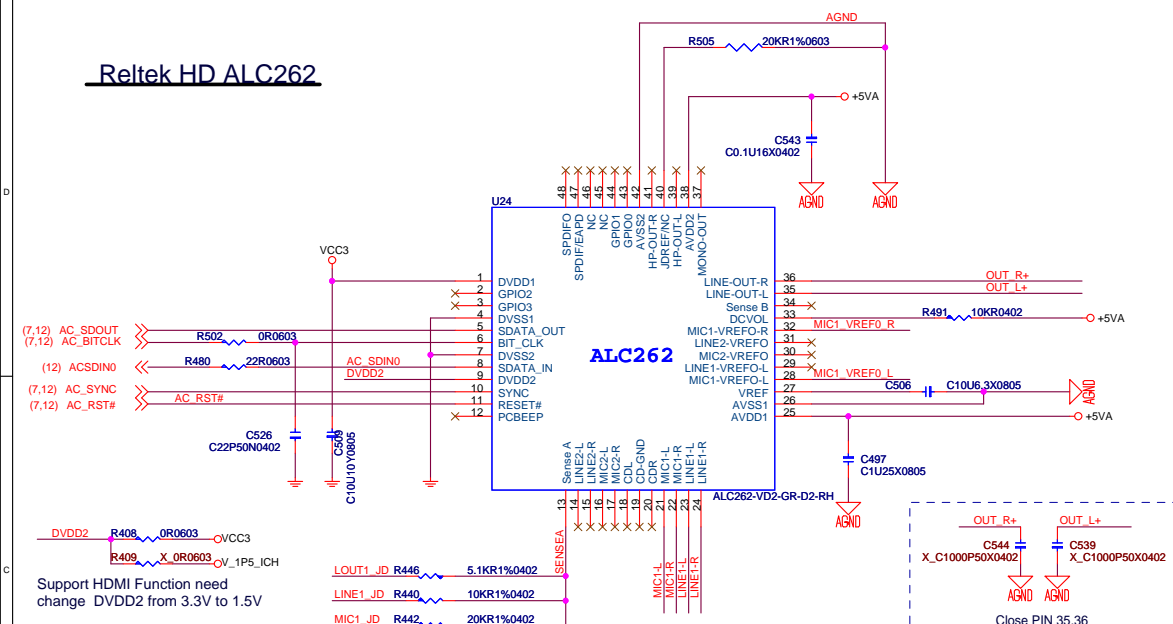


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MS-7428N1

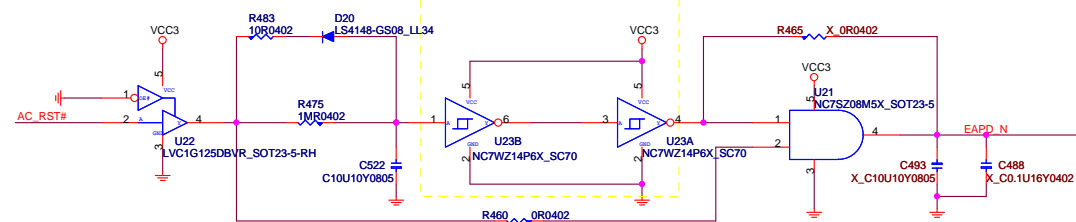
Size Custom	Document Description Broadcom-BCM5784M	Rev 0B
Date: Thursday, July 03, 2008		Sheet 28 of 35

Reltek HD ALC262

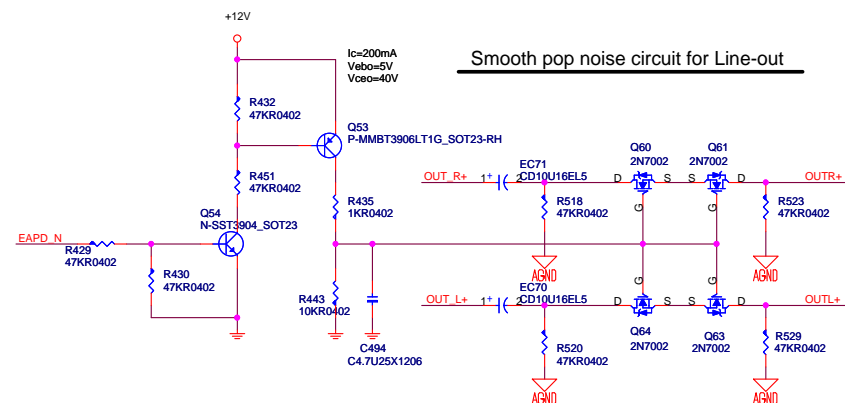


POP noise circuit

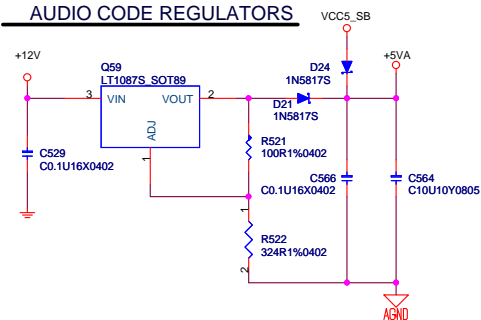
06/18/2008 update - To change buffer type to schmitt trigger*2



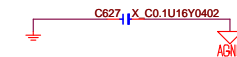
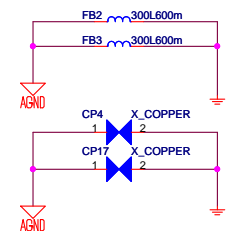
Smooth pop noise circuit for Line-out



AUDIO CODE REGULATORS



Rev.0B change R522 from 348R to 324R :
 $V_o = 1.25 \times [1 + (324/100)] + [55^{\circ}300 \times 10e-6] = 5.3V$
 Voltage drop from D21=0.1~0.25V
 $+5VA = 5.3V - 0.25V = 5.05V$



MICRO-STAR INT'L CO.,LTD

MS-7428N1

Size

Document Description

	HD Audio AL
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Rev	
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Sheet	29	of	35
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ICH10

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	PECI_REQUEST# function,Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK21
GPIO 2	I/O	GPI	PIRO#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPI	PIRO#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPI	PIRO#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPI	PIRO#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPI	Pull-up to VCC3_SB with 10K	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE/GPIO9, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPI	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	NC.	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPI	SIO_PME# connect to SIO,pull-up VCC3_SB with 10k	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPI	SIO_SMI# connect to SIO,Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# for CK505 iAMT,not use	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	pull-up VCC3 with 10K.	VCC3	UNMUXED	M2
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	K1
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRO1#	LDRO_1# pull-up VCC3 with 10K(Not Use)	VCC3	MUXED	J3
GPIO 24	I/O	GPO	SPI_HOLD_GPO#,not use	3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# for CK505 iAMT,not use	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE#	3.3V_SB		C11
GPIO 27	I/O	GPO	LPM_LAN ,control VCC3_SBLAN power	3.3V_SB		A11
GPIO 28	I/O	GPO	SPI_WP#	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#2 connect to USB connector (Port6,7)	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		M1
GPIO 32	I/O	GPO	PROHOT# for NEC Economy mode	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	NC	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	NC	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	SATACLKREQB_GP35,not use	VCC3		L1
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC0#	OC#0 connect to USB connector (Port0,1,2,3)	3.3V_SB		N3
GPIO 41	I/O	OC1#	OC#1 connect to USB connector (Port4,5)	3.3V_SB		P7
GPIO 42	I/O	OC1#	OC#1 connect to USB connector (Port4,5)	3.3V_SB		R7
GPIO 43	I/O	OC2#	OC#2 connect to USB connector (Port6,7)	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#3 connect to USB connector (Port10,11)	3.3V_SB		T7/P1
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping ,not use	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#	VCC3	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3#(Not Use)	VCC3	MUXED	F7
GPIO 56	I/O	GPI	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPI	Pull-up to VCC3_SB with 10K directly	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS#(Not Use) , SPI_CS1_F#(Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector (Port0,1,2,3)	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	LINKALERT, pull-up to VCC3_SB with 10K	3.3V_SB		F18
GPIO 61	I/O	GPO	LPCPD#,connect to SIO and TPM	3.3V_SB	MUXED	R1
GPIO 62	I/O	GPO	(Not Use)	3.3V_SB	MUXED	R5
GPIO 63	I/O	GPO	(Not Use)	3.3V_SB		G17
GPIO 72	I/O	GPO	BATTLOW#, pull-up to VCC3_SB with 10K	3.3V_SB		C13

PCI Configuration

DEVICE	MCP1 INT Pin	REQ# /GNT#	IDSEL	CLOCK
PC11	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PC12	PIRQ#B PIRQ#D PIRQ#C PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDR2 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A2/SCLK_A2#
DIMM 2	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#
DIMM 3	0A0H	SCLK_A0/SCLK_A0# SCLK_A2/SCLK_A2#
DIMM 4	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#

SIO - SMSC-5617C Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP76	53	GPIO_KB	OUTPUT
GP42	27	SIO_SMI#	OUTPUT
GP41	77	SIO_PME#	OUTPUT
GP23	21	LAN_DISABLE	OUTPUT

Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
J1	(1-2)short: Normal	(1-2)Open: Clear PW



PCB

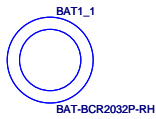


CPU Retention Mouldle



CPU Retention W/screw&washer

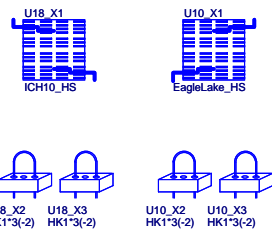
Battery



Jumper



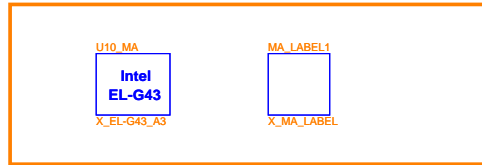
Heatsink



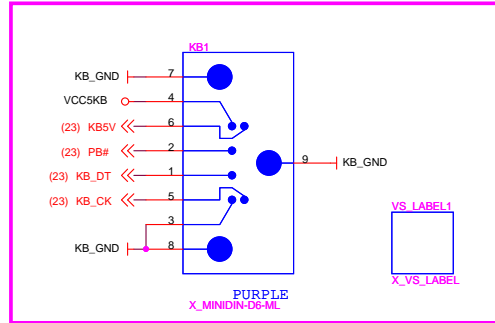
BIOS Label



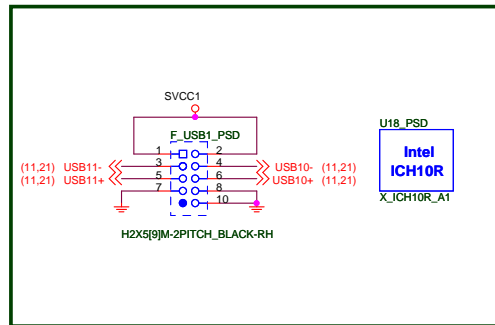
Ropros-Mate



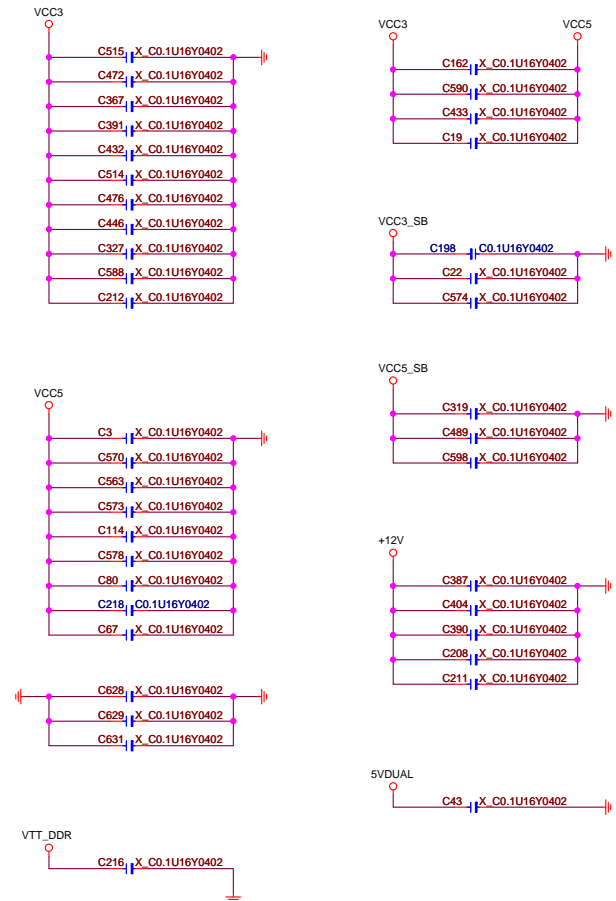
Ropros-VS(G45/G43)



Poseidon-E



EMI SUGGESTION



LGA775-CPU		
1.15V - 1.50V Core	-	60A
1.1V FSB Vtt	-	4.6A

Eaglelake (GMCH)		
1.1V FSB_VTT	-	1.2 A
1.1V Core TBD (USE LB)	-	13.8A
1.1V DMI/PCI Exp.	-	2.47 A
1.1V Vcc CL	-	3A
1.8V VCC_DDR	-	3.33A
1.8V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA

ICH10		
1.1V DMI	-	41 mA
1.1V Core	-	1.16A
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262VD		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

IDTCV184-2		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

BCM5784M		
3.3V_SB I/O & LED	-	15.5mA
1.2V ANALOG	-	0.418A

ISL6312		
VCCP VRD 11-cfg06		
1.15V-1.50V 60A(65W)		
3-Phase Switch		

W83310DS		
VTT_DDR		
0.9V Linear 1.2A		

MS11+ SW-Power		
VCC_DDR		
1.8V PWM 20.8A		

MS11+ SW-Power		
V_1P1_CORE		
1.1V PWM 20.47A		

MS7 CONTROLLER		
V_1P5_ICH		
1.5V Linear 2A		
VCC3_SB		
3.3V Linear 1.5A		
5VDUAL		
5V Switch 5A		
5VSB Switch 500mA		
5VDUAL1		
5V Switch 15A		
5VSB Switch 500mA		
5VDIMM		
5V Switch 15A		
5VSB Switch 500mA		

DDRII x4 & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

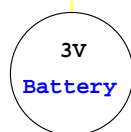
PCI slot x1		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

PCI Express x 1 slot *2		
+12V	-	0.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

USB x8		
+5V (S0,S1)	-	6.0A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

5VAUD		
5V		
500mA		



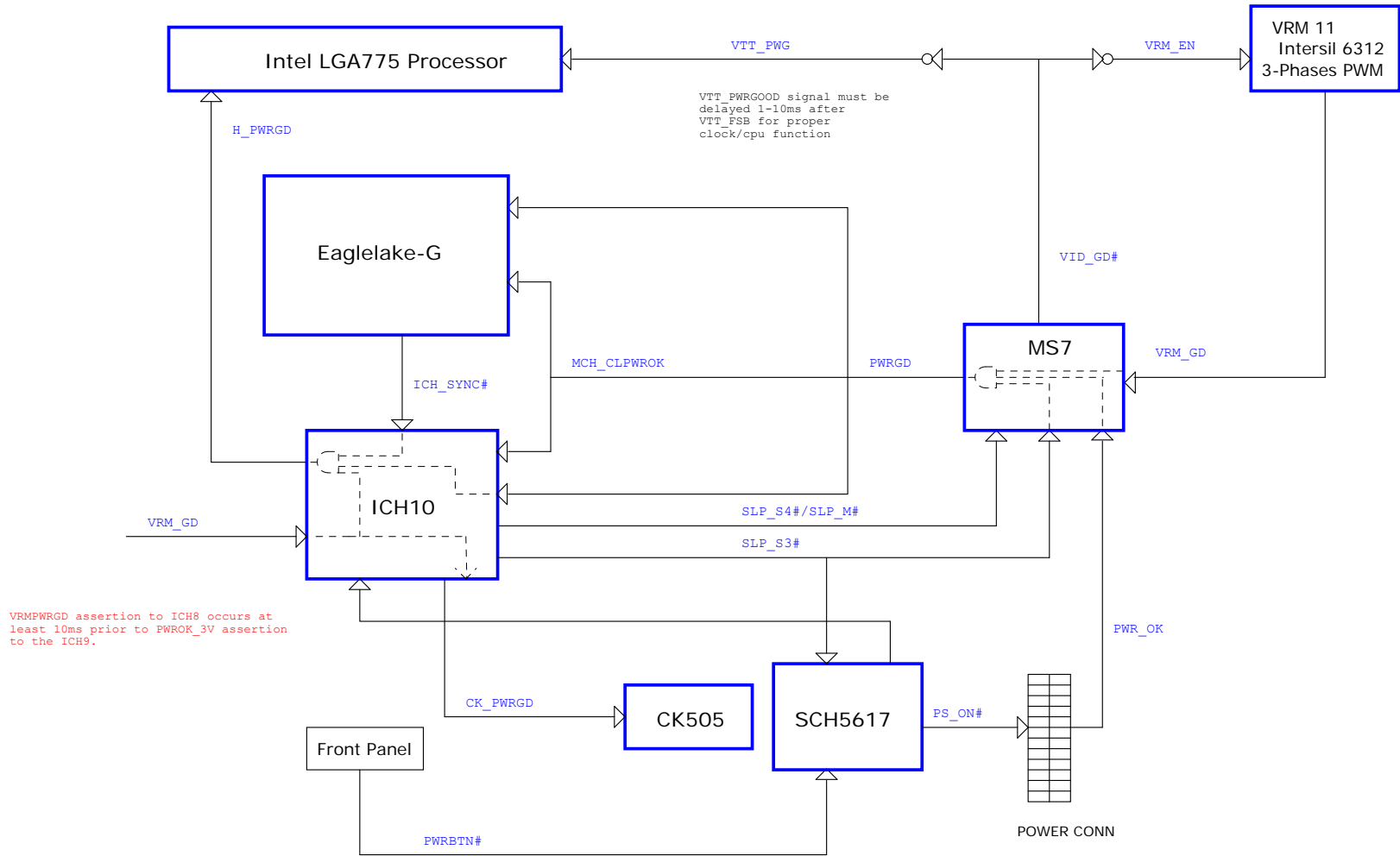
+12V	
ATX 2x2	

+5V	+3.3V	+5VSB	+12V
ATX POWER			

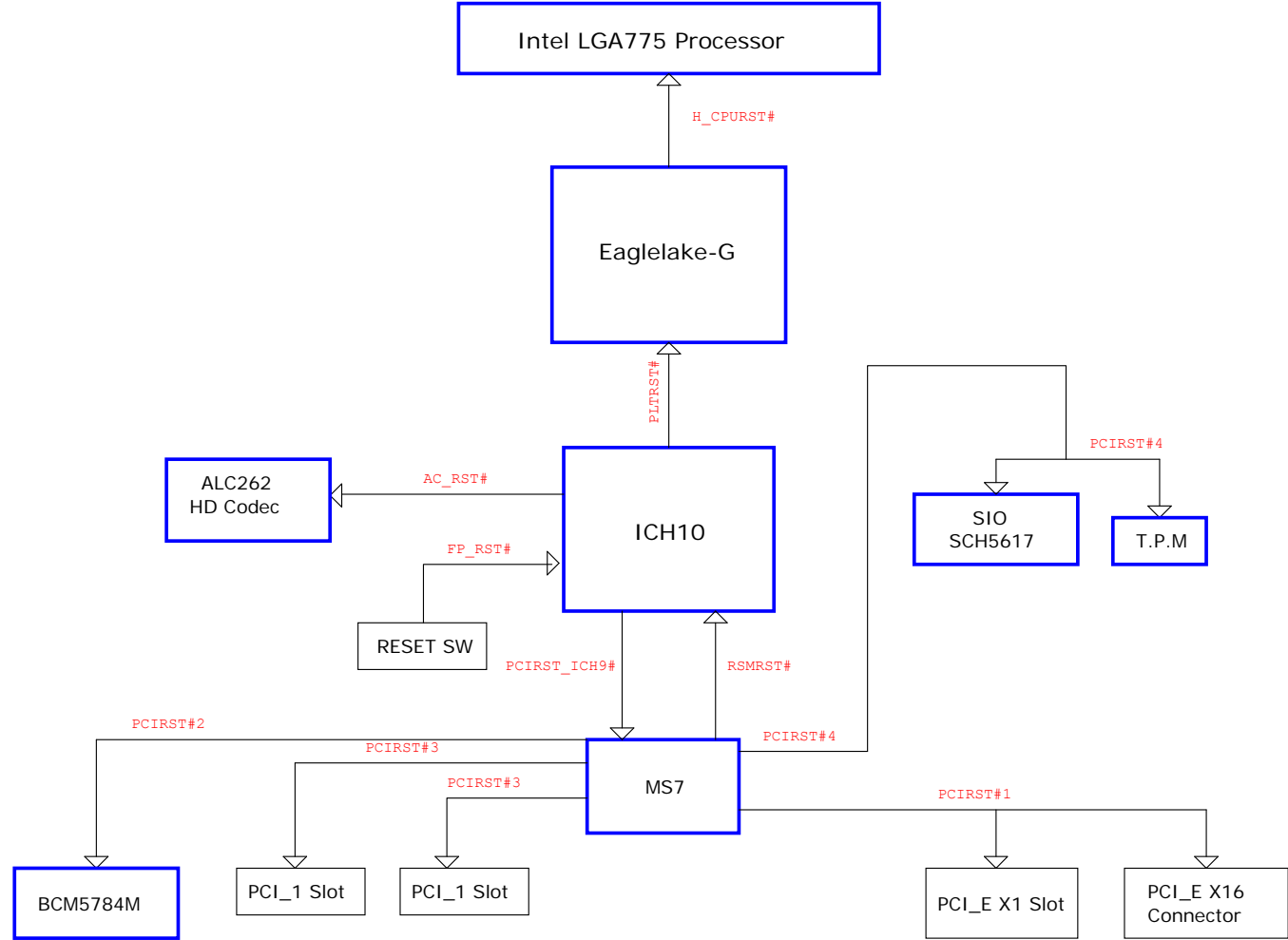


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PWROK MAP



RESET MAP



0A change to 0B : (2008/06/25)

Page10.
* To change all of assembly level of C602/C611/C609/C606... from bottom side to top side and stuff most of theses components. (EE)

Page11.
* No stuff R500 to set HW strap to PCIE[X1]*4. (EE)
* To chage the USB singnal of MRC from port8&9 to port6&7. (BIOS request)

Page12.
* To remove JCI1 and stuff R396. (No need for NECP)

Page13.
* To change assembly level of C617/C620/C646/C615/C621 from bottom side to top side and stuff these components. (EE)
* To change R481 from 10ohm to 100ohm & C519 from 0.1uf to 1uf. (Intel MOW update)
card. (EE)

Page16.
* To change C426/C438 from 27P50N to 47P50N to correct frequency of Y3. (EE)

Page21.
* To chage the USB singnal of MRC from port8&9 to port6&7. (BIOS)
* To change L37/L38/L39/L40 from 120ohm to 90ohm. (EE)
* To swap USB port0/1/2/3 for real port because ball out issue of port 6/7/8/9 has been changed. (Layout/EE)

Page22.
* To change L5/6/7 from 68nH to 82nH; C143/151/154 from 10P to 12P; C144/152/155 from 10p to 6.8p; Stuff C249/257/253 with 10P. (EMI/EE)
* No stuff C129/C132 for H/V SYNC to solve undershoot ringback over 0.5V. (EE)

Page23.
* To pull up VCC3 with 10KR for LPCPD# of TPM. (Infineon's AP note for ICH10)

Page24.
* To add a 10KR pull high resister for VRM_GD. (EE)
* To change U3 from ISL6312CRZ-T to ISL6312CRZ-TR5312. (New manufacture process of PWM IC)
* To change R12 from 22KR to 15KR1%; change R19 from 200R1% to 340R1%; change R62 from 120KR to 105KR1%; change COIL4 from 1.2u/18A to 1.1u/27A. (PWR team)


Page25.
* To add Posister circuit for thermal sense. (NECP request)
* To add V_FSB_VTT select circuit for Yorkfield CPU and change this power to CPU/MCH/ICH which is releated it. (Intel Eaglelake MCH FSB margin improvement)
* No stuff R413, reserve only. (EE)
* To remove R209/R516, connect RAM_DRV to Q32/Q62 directly. (EE)

Page26.
* To change CHOKE1/CHOKE3 from 1.2u/8A to 1.2u/15A and change CHOKE2/CHOKE4 from 1.2u/18A to 1.1u/27A. (PWR team)

Page28.
* To change the GPIO of LAN_Disable from ICH-GPIO12 to SIO-GPIO23. (GPIO12 only can setting by FITC tool)
* To change U15 from AT45DB011B-SU to AT45DB011B-SH. (New manufacture process)
* To remove 8 EMI capacitor. (EMI/EE)

Page29.
* To remove components(JAUD1/EC75,76...) which related to front audio. (No need for NEC_CAP)
* To change R521 from 100R5% to 100R1% and change R522 from 348R1% to 324R1%. (EE, keeping +5VA level correct)
* To change U23 from buffer(LVC1G125) to Schmitter-Trigger(7WZ14)*2 type. (NECP)

Page31.
* To add EMI capacitors C208/C211/C212/C216.

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